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Research Article

WIDE FAN-IN GATES FOR COMBINATIONAL CIRCUITS USING CCD

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ABSTRACT

In order to improve the performance and to reduce the power consumption of integrated circuits, supply voltage is reduced often. This results in low power consumption but introduces some problems such as less noise immunity and exponential increase in sub-threshold leakage current. Hence the major concerns in modern integrated circuits are the designing circuits which are robust to noise and reducing sub-threshold leakage current.This becomes a problem especially in the wide fan-in integrated circuits.For this purpose a new type of domino circuit is proposed. This domino circuit is very useful in improving the noise robustness of the integrated circuit and also in reduction of sub-threshold leakage current. This technique is called current-comparison-based-domino (CCD)circuit for wide fan –in applications in ultradeep sub-micrometer technology. In the existing system current-comparison-based-domino (CCD)circuit technique is applied for wide fan-in OR gate. In the proposed work current-comparison-based-domino (CCD) circuit technique will be applied for wide fan-in universal gates such as NAND and NOR gates. Hence the proposed circuit technique decreases the parasitic capacitance on the dynamic node which yields a small keeper for wide fan-in gates to implement fast and robust circuit. The performance of the technique will be assessed using TSPICE.

Keywords: Domino logic, leakage-tolerant, noise immunity, wide fan-in, Wallace Multiplier.

INTRODUCTION

Scaling is the primary thrust behind the advancement of CMOS technology[1]. The increased leakage currents and the enhanced device sensitivity to process parameter fluctuations have become the primary barriers against further CMOS technology scaling. The rapid integration of VLSI circuit is due to the increased use of portable wireless systems with low power budget and microprocessors with higher speed[2]. To achieve high speed and lower power consumption transistor technology and power supply must be scaled down simultaneously[3]. As the technology scales down the threshold voltage (V*th*) of the transistor also lowers in the same proportionate. Scaling of threshold voltage results in exponential increase of sub threshold leakage current in the evaluation transistor and makes the domino logic less noise immune. The main source of noise in deep-submicron circuit is mainly due to the higher leakage current, crosstalk, supply noise and charge sharing, while noise at the input of the evaluation transistor may increases due to increased crosstalk. In domino logic scaling the supply voltage and capacitance of dynamic (pre-charge) node reduces the amount of charge stored at the dynamic node[4]. Due to all these concurrent factors, the noise immunity of domino gate substantially decreases with technology scaling. The leakage immunity is more problematic in high fan-in domino circuits because of larger leakage due to more parallel evaluation paths[5]. Since the leakage current is proportional to the fan-in domino OR gate, the noise immunity also decreases with fan-in increases. Leakage and noise immunity are major issues for the wide fan-in domino OR logic, because the evaluation transistor are all in parallel, leaking the charge from precharge node. The most popular dynamic logic is the conventional standard footless domino circuit. In this design, a pMOS keeper transistor is employed to prevent any undesired discharging at the dynamic node due to the leakage currents and charge sharing of the pull-down network (PDN) during the evaluation phase, hence improving the robustness[6]. Keeper transistor upsizing is a conventional method to improve the robustness of domino circuits. However, as the keeper transistor is upsized the contention between the keeper transistor and the evaluation network increases in the evaluation phase. This causes an increase in the evaluation delay of the circuit, increase in power consumption and degradation of performance[7]. Therefore, to improve noise and leakage immunity, keeper upsizing is used as a compromise between delay and power. The keeper ratio *K* is defined as

$$K = \frac{\mu_p(\frac{W}{L})_{Keeper-transistor}}{\mu_n(\frac{W}{L})_{Evaluation-transistor}}$$

Where *W* and *L* denote the transistor size, and μ_n and μ_p are the electron and hole mobilities respectively. A new current-comparison-based domino (CCD) circuit for wide fan-in applications in ultradeep submicrometer technologies is proposed. The leakage power of 4*4 Wallace tree multiplier is reduced by replacing half adders by full adders. Here multiplier is designed by current comparison based domino logic full adders. From the simulation results, it can be concluded that the total leakage power has been drastically reduced by reducing half of the dynamic power dissipation. The rest of this paper is arranged as follows. After the literature review in Section II, the proposed circuit is described in Section III. Section IV includes simulation results for the proposed circuit using TANNER EDA tool version compared with other conventional circuits. Section V concludes the results[8].

VARIOUS DOMINO LOGICS

Several circuit techniques are proposed in the literature to address these issues. In the first category, circuit techniques change the controlling circuit of the gate voltage of the keeper such as conditional-keeper domino (CKD), high speed domino(HSD), conditional keeper current comparison domino(CKCCD) as shown in Fig. 1(a), 1(b) and 1(c) respectively.

In the second category, designs including the proposed designs change the circuit topology of the footer transistor or reengineer the evaluation network such as diode footed domino (DFD) and diode-partitioned domino (DPD) as shown in Fig. 1(d) and (e), respectively[9].

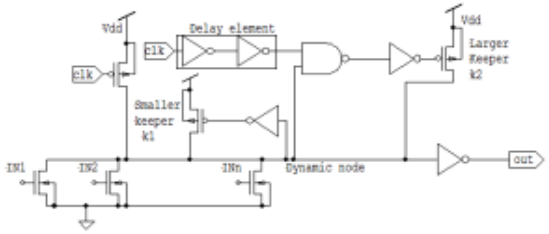

Figure 1 a): CKD

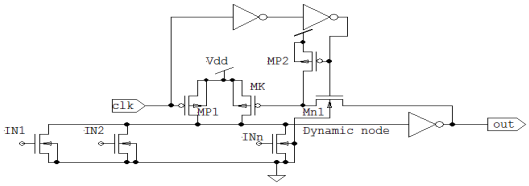

Figure 1 b): HSD

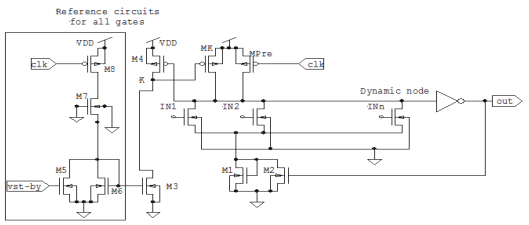

Figure 1 c): CKCCD

The drawbacks analysed with the existing works are increase in leakage current, noise immunity, decrease in contention current robustness, power consumption, delay etc.,

The multiplier is designed using standard domino logic style. The 4*4 Wallace tree multiplier with full adder method replaces the full adders in the place of half adders. So there is no need for separate final summing unit.

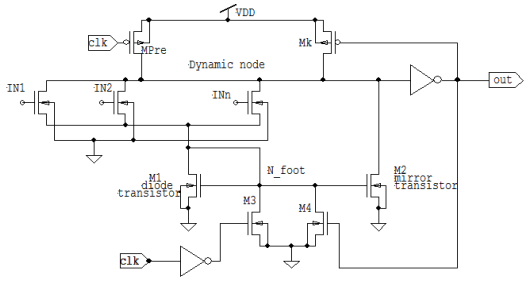

Figure 1 d): DFD

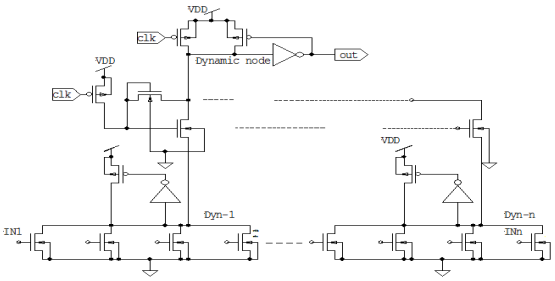

Figure 1 e): DPD

Hence the total leakage power is reduced. A 4*4 Wallace tree multiplier is designed using current comparison based domino logic full adders.4*4 Wallace multiplier has 12 full adders where all these full adders are replaced by current comparison based domino logic full adders[10].

PROPOSED CCD IN WALLACE TREE MULTIPLIER CCD DESIGN

Considering the wide fan-in gates, the speed is dramatically decreased since the capacitance of the dynamic node is large. Even though, upsizing the keeper transistor can improve noise robustness, power consumption and delay are increased due to large contention. These problems could be resolved if the PDN implements logical function, is separated from the keeper transistor by using a comparison stage in which the current of the pull-up network (PUN) is compared with the worst case leakage current. This idea is illustrated in Fig. 2(a). where PUN is used instead of PDN.

Transistor *MK* is added in series with the reference current to reduce power consumption when the voltage of the output node has fallen to ground voltage. Another important issue is the generation of reference voltage, which is the correct variation of the reference current according to the process variations in order to maintain the robustness of the proposed circuit.

In the proposed circuit, effects of any threshold voltage variation on the voltage of nodes A and B [in Fig. 2(b)] is important because it directly affects the speed of the gate, and consequently power consumption and noise immunity[11].

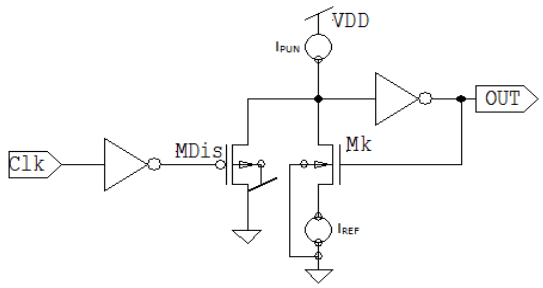

Figure 2 a): Concept of proposed CCD design

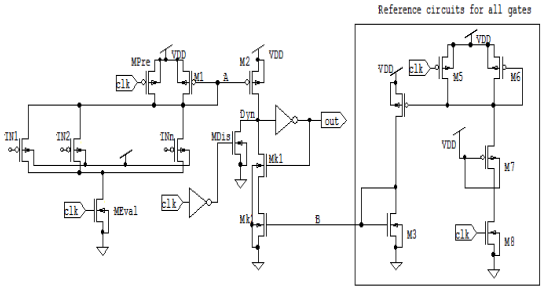

Figure 2 b): Implementation of wide fan-in OR gate using CCD

Predischarge Phase

Input signals and clock voltage are in high and low levels, respectively, [CLK = "0", CLK = "1" in Fig. 2(b)] in this phase. Therefore, the voltages of the dynamic node (Dyn) and node A have fallen to the low level by transistor MDis and raised to the high level by transistor Mpre, respectively. Hence, transistors Mpre, MDis, Mk1, and Mk2 are on and transistors M1, M2, and MEval are off. Also, the output voltage is raised to the high level by the output inverter.

Evaluation Phase

In this phase, clock voltage is in the high level [CLK = "1", CLK = "0" in Fig. 2(b)] and input signals can be in the low level. Hence, transistors Mpre and MDis are off, transistorM1, M2, Mk2, and MEval are on, and transistor Mk1 can be come on or off depending on input voltages. Thus, two states may occur. First, all of the input signals remain high. Second, at least one input falls to the low level. In the first state, a small amount of voltage is established across transistor M1 due to the leakage current. Although this leakage current is mirrored by transistor M2, the keeper transistors of the second stage (Mk1 and Mk2) compensate this mirrored leakage current. It is clear that upsizing the transistor M1 and increasing the mirror ratio (M) increase the speed due to higher mirrored current at the expense of noise-immunity degradation.

WALLACE TREE MULTIPLIER

A 4*4 Wallace tree multiplier is designed using current comparison based domino logic full adders.4*4 Wallace multiplier has 12 full adders, where all these full adders are replaced by current comparison based domino logic full adders. By these adders dynamic power dissipation in the multiplier is reduced such that half of the total leakage power in the 4*4 Wallace tree multiplier is reduced. The concept of current comparison based domino logic is shown in figure 3.a.

In this logic pull down network implements the logical function and it is separated from the keeper transistor by current comparison stage. This stage compares the pull up network current with the worst case leakage current. Here transistor M_k is added in series with the reference current to reduce power dissipation when the voltage of the output node has fallen to ground voltage. An important issue in this logic is the generation of reference voltage, which is the correct variation of the reference current according to the process variations to maintain the functionality of the proposed circuit. Generally process variations are due to random and systematic parameter fluctuations. Here the full adder is designed by current comparison based domino logic which uses the replica keeper current method to track the leakage current i.e., systematic process variation as shown in Fig 3.

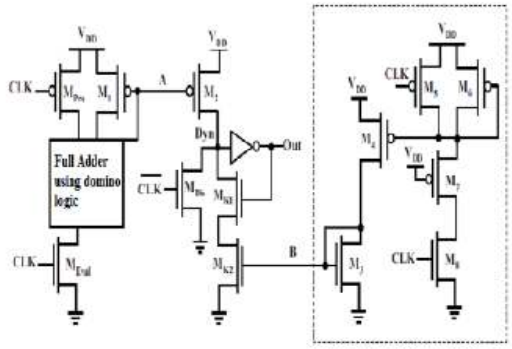

Figure 3: Implementation of full adder using current comparison based domino logic

SIMULATION RESULTS AND COMPARISONS

The proposed circuit was simulated using EDA Tanner tool with 180nm technology. Figure 4 shows the graphical illustration of the comparison of power consumption between various domino logics. It shows a reduction in normalized power consumption from 10% to 39% compared to the SFLD. The comparison of delay of various domino logic for wide fan-in OR gates are illustrated in Figure 5. The results obtained indicate that 1.77 to 1.92 times improvement over the SFLD, indicating that the proposed circuit has a less delay compared with the rest. The relationship between the number of inputs and reduction in the delay and power consumption of the proposed circuit, which is normalized to SFLD counterparts are shown in Fig 6. As shown in the illustration, the proposed circuit has lower power consumption and delay if the number of inputs is greater than 16 and 32.

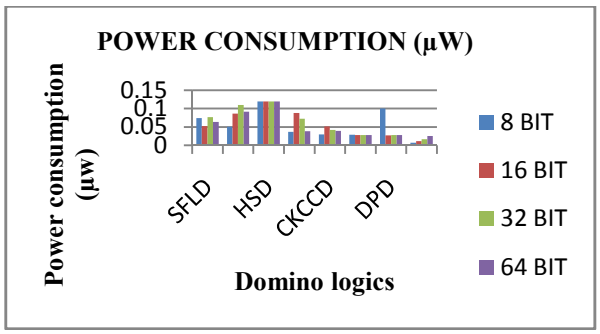

Figure 4: Comparison of Power consumption of the domino circuits in 180nm technology

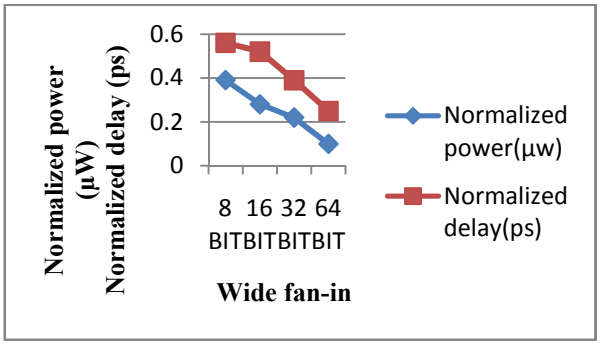

Figure 6: Relationship between normalized delay and power consumption of proposed circuit in terms of number of inputs

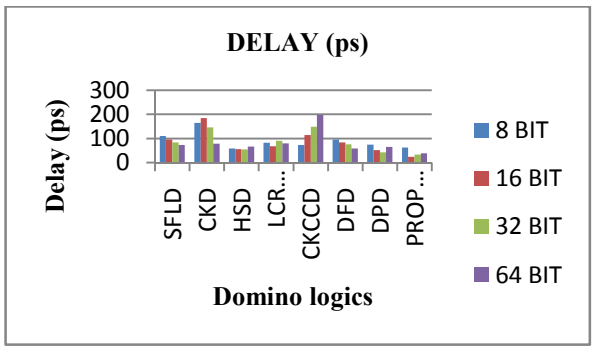

Figure 5: Comparison of Delay of the domino circuits in 180nm technology

To consider the process variations, variations of delay and power consumption of a 64 bit wide fan-in OR gate, which is implemented in the proposed circuit and the other circuits simulated via Monte Carlo simulations of MICROWIND are shown in Table 1 and Table 2. In these tables, μ and σ are the mean value and standard deviation value of the given variable, respectively.

Figure 8 shows the schematic of CCD in full adder (CCDFA).The full adder operation equations presented below can be stated as follows: given the three 1-bit inputs A, B and Cin which calculate two 1-bit outputs Sum, for sum and Cout for carry out.

$$Sum = A\ XOR\ B\ XOR\ C_{in}$$

$$C_{out} = \text{A XOR B} + \text{B XOR } C_{in} + C_{in}$$

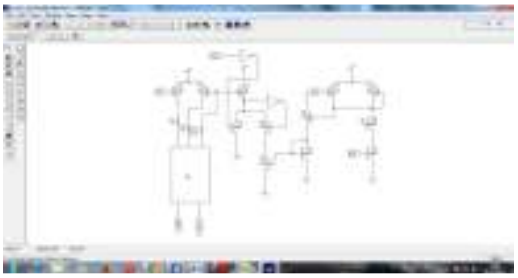

Figure 7: Schematic of full adder using current comparison domin

Table 1: Effect of Threshold Fluctuations Due to Process Variations on Power for 64-Bit or Gate

Voltage Variation	Variable	SFLD	CKD	HSD	LCR KEEPER	CKCCD	DFD	DPD	PROPOSED CCD
1	μ Power (mW)	0.0536	0.2032	0.0824	0.0608	0.0728	0.0505	0.0762	0.0416
	σ Power (mW)	0.0114	0.0339	0.0109	0.0132	0.0055	0.0013	0.0147	0.0096
1.2	μ Power (mW)	0.1675	0.4249	0.1824	0.1637	0.1222	0.0825	0.1716	0.0896
	σ Power (mW)	0.0457	0.0549	0.0256	0.0205	0.0052	0.0042	0.0188	0.0099
2	μ Power (mW)	1.1732	3.485	0.2409	0.14	0.701	0.4459	1.6341	0.5024
	σ Power (mW)	0.1658	0.231	0.071	0.1643	0.068	0.0265	0.1867	0.616
2.4	μ Power (mW)	2.6559	7.2853	2.6318	2.7264	1.2291	0.8799	3.3821	0.9329
	σ Power (mW)	0.3327	0.4679	0.1024	0.2608	0.0577	0.0589	0.4695	0.0896

Table 2: Effect of Threshold Fluctuations due to Process Variations on Delay for 64-Bit or Gate

Voltage Variation	Variable	SFLD	CKD	HSD	LCR KEEPER	CKCCD	DFD	DPD	PROPOSED CCD
1	μ Delay (ns)	0.13	0.495	0.307	0.331	0.351	0.662	0.239	0.129
	σ Delay (ns)	0.234	0.3166	0.35	0.321	0.3509	0.2652	0.3137	0.2853
1.2	μ Delay (ns)	0.378	0.522	0.613	0.194	0.608	0.368	0.48	0.372
	σ Delay (ns)	0.39	0.0411	0.403	0.315	0.2626	0.1411	0.3763	0.2733
2	μ Delay (ns)	0.329	0.422	0.592	0.013	0.257	0.13	0.528	0.538
	σ Delay (ns)	0.334	0.0107	0.0166	0.026	0.0272	0.2436	0.024	0.0213
2.4	μ Delay (ns)	0.318	0.436	0.577	0.009	0.297	0.061	0.535	0.435
	σ Delay (ns)	0.318	0.006	0.0045	0.0192	0.045	0.098	0.0156	0.0269

Figure 7 shows the design of current comparison domino based full adder in Wallace tree multiplier and simulated using EDA Tanner tool with 180nm CMOS process technology.

Table 3 shows the comparison of power consumption of Wallace tree multiplier using various circuit techniques with

the proposed current comparison based Wallace tree multiplier.

The proposed 4*4 Wallace tree multiplier using current comparison based domino logic full adders was simulated using TANNER EDA which shows a relative power reduction when compared to the 4*4 Wallace tree multiplier using standard full adders.

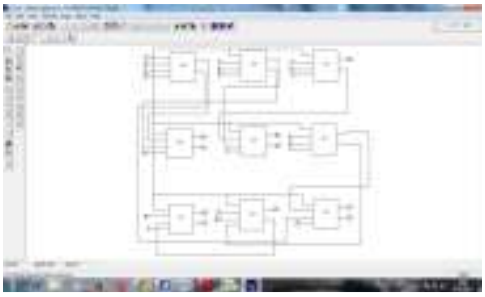

Figure 8: Schematic of Wallace tree multiplier using current comparison domino

Table 3: Comparison of Power Consumption of Multipliers using various Domino Logics

	SFLD full adder based multiplier	CKD full adder based multiplier	HSD full adder based multiplier	LCR Keeper full adder based multiplier	CKCCD full adder based multiplier	DFD full adder based multiplier	DPD full adder based multiplier	Proposed CCD full adder based multiplier
Power dissipation (mW)	5.273	14.116	5.6	7.654	26.405	15.124	20.652	3.0331

CONCLUSION

A new circuit design that we called CCD was proposed. The main goal was to make the domino circuits more robust and with low leakage without significant performance degradation or increased power consumption. Relative decrease in power consumption and delay is achieved by using current comparison domino. The leakage power of 4*4 Wallace tree multiplier is reduced by replacing half adders by full adders. In order to reduce this leakage power, we present current comparison based domino logic 4*4 Wallace tree multiplier. From the simulation results, it can be concluded that the total leakage power has been drastically reduced by reducing half of the dynamic power dissipation.

REFERENCES

1. Peiravi A, Mohammad A. Current-Comparison-Based Domino: New Low-Leakage High-Speed Domino Circuit for Wide Fan-In Gates in IEEE Transactions On Very Large Scale Integration (VLSI) Systems. 2013; 21(5).
2. Naveen R, Thanushkkodi K, saranya C. Leakage Power Reduction In Wallace Tree Multiplier Using Current Comaprison Based Domino Logic Full Adders in Journal of Theoretical and Applied Information Technology. 2013; 55(1).
3. Wang L, Krishnamurthy R, Soumyanath K, Shanbhag N. An energy-efficient leakage-tolerant dynamic circuit technique in Proc. Int.ASIC/SoC Conf. 2000: 221.
4. Predictive Technology Model (PTM). 16 nm High Performance V2.1 Technology of PTM Model. 2012; Available:http://www.eas.asu.edu/ptm
5. Mahmoodi H, Roy K. Diode-footed domino: A leakage-tolerant high fan-in dynamic circuit design style," IEEE Trans. Circuits Syst. I Reg. Papers. 2004; 51(3): 495.
6. Alvandpour, Krishnamurthy R, Sourrty K, Borkar SY. A sub-130-nm conditional-keeper technique IEEE J. Solid-State Circuits: 2002; 37(5): 633.
7. Anis MH, Allam MW, Elmasry MI. Energy-efficient noise-tolerant dynamic styles for scaled-down CMOS and MTCMOS technologies IEEE Trans. Very Large Scale (VLSI) Syst: 2002; 10(2); 71.
8. Lih Y, Tzartzanis N, Walker WW. A leakage current replica keeper for dynamic circuits IEEE J. Solid-State Circuits:2007; 42(1); 48.
9. Peiravi, Asyaei M. Robust low leakage controlled keeper by current-comparison domino for wide fan-in gates, integration.VLSI J:2012; 45(1): 22.
10. Suzuki H, Kim CH, Roy K. Fast tag comparator using diode partitioned domino for 64-bit microprocessorsIEEE Trans. Circuits Syst: 2007; 54(2): 322.
11. Bowman K, Duval SG, Meindl JD. Impact of die-to-die and within-die parameter fluctuations on the maximum clock frequency distribution for giga scale integration. IEEE J. Solid-State Circuits: 2002; 37(2): 183.

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