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Research Article

A POWER EFFICIENT CAM DESIGN USING MODIFIED PARITY BIT MATCHING TECHNIQUE

Karthik M[1*], Jegan RR[2], Prasanna Venkatesan GKD[3]

[1]ME VLSI student PGP college of Engineering and Technology Nammakkal,Tamilnadu, India.
[2]AP, PGP college of Engineering and Technology Nammakkal,Tamilnadu, India
[3]Vice Principal, Professor and Head/ECE, PGP College of Engineering & Technology, Namakkal. Tamilnadu, India

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*Corresponding Author: **Karthik M**
ME VLSI student PGP college of Engineering and Technology Nammakkal,Tamilnadu, India.

ABSTRACT

Content-addressable memory (CAM) is a hardware table that can compare the search data with all the stored data in parallel. Due to the parallel comparison feature where a large amount of transistors are active on each lookup, however, the power consumption of CAM is usually considerable. Thus, robust, high-speed and low-power sense amplifiers are highly sought-after in CAM designs. In this paper, we introduce a modified parity bit matching that leads to delay reduction, area and power overhead. The modified design minimizes the searching time by matching the store bit from most significant bit instead of matching all the data's present in the row. Furthermore, we propose an effective gated-power technique to reduce the peak and average power consumption and enhance the robustness of the design against process variations.

Keywords: CAM, Parity CAM, ATM Controller, VPI/VCI

INTRODUCTION

Content-addressable memories (CAMs) are hardware search engines that are much faster than algorithmic approaches for search-intensive applications. CAMs are composed of conventional semiconductor memory (usually SRAM) with added comparison circuitry that enables a search operation to complete in a single clock cycle. The two most common search-intensive tasks that use CAMs are packet forwarding and packet classification in Internet routers[1].

We survey recent developments in the design of large-capacity content-addressable memory (CAM). A CAM is a memory that implements the lookup-table function in a single clock cycle using dedicated comparison circuitry. CAMs are especially popular in network routers for packet forwarding and packet classification, but they are also beneficial in a variety of applications that require high-speed table lookup. The main CAM-design challenge is to reduce power consumption associated with the large amount of parallel active circuitry, without sacrificing speed or memory density. In this paper, we review CAM- design techniques at the circuit level and at the architectural level. At the circuit level, we review low-power match line sensing techniques and search line driving approaches. At the architectural level we review three methods for reducing power consumption[2].

PARITY CAM

Content-addressable memory (CAM) is frequently used in applications, such as lookup tables, databases, associative computing, and networking, that require high-speed searches due to its ability to improve application performance by using parallel comparison to reduce search time. Although the use of parallel comparison results in reduced search time, it also significantly increases power consumption. In this paper, we propose a Block-XOR approach to improve the efficiency of low power precomputation-based CAM (PB-CAM). The major contribution of this paper is that it presents theoretical and practical proofs to verify that our proposed Block-XOR PB-CAM system can achieve greater power reduction without the need for a special CAM cell design[3].

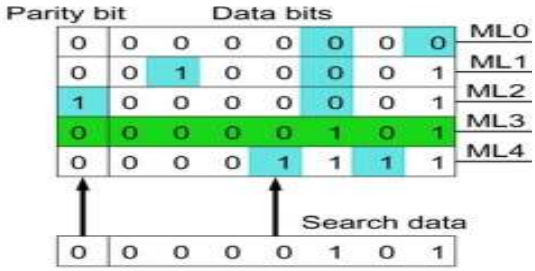


Figure 1: Parity bit based CAM

A content-addressable memory (CAM) is a critical device for applications involving asynchronous transfer mode (ATM), communication networks, LAN bridges/switches, databases, lookup tables, and tag directories, due to its high-speed data search capability. ACAM is a functional memory with a large amount of stored data that simultaneously compares the input search data with the stored data. Once matching data are found, their addresses are returned as output as shown in Fig. 1. The vast number of comparison operations required by CAMs consumes a large amount of power. In the past decade, much research on energy reduction has focused on the circuit and technology domains[1] provides a comprehensive survey on CAM designs from circuit to architectural levels). Several works on reducing CAM power consumption have focused on reducing match-line power[2-4]. Although there has been progress in this area in recent years, the power consumption of CAMs is still high compared with RAMs of similar size. At the same time, research in associative cache system design for power efficiency at the architectural level continues to increase. The filter cache[5,6] and location cache techniques[7] can effectively reduce the power dissipation by adding a very small cache. However, the use of these caches requires major modifications to the memory structure and hierarchy to fit the design. Pagiamtzis et al. proposed a cache-CAM (C-CAM) that reduces power consumption relative to the cache hit rate. Lin et al. presented a ones-count pre computation-based CAM (PB-CAM) that achieves low-power, low cost, low-voltage, and high-reliability features. Although Cheng[1] further improved the efficiency of PB-CAMs, the approach proposed requires considerable modification to the memory architecture to achieve high performance. Therefore, it is beyond the scope of the general CAM design. Moreover, the disadvantage of the ones count PB-CAM system is that it adopts a special memory cell designfor reducing power consumption, which is only applicable to the ones count parameter extractor[4].

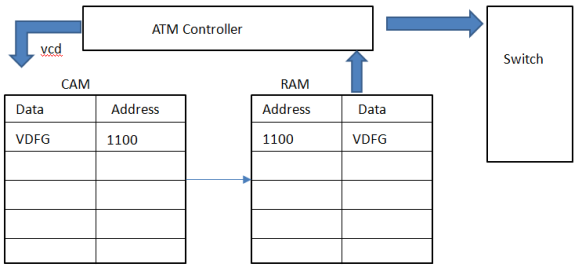


Figure 2: ATM Controller Block Diagram

CAMs can be used in Asynchronous Transfer Mode (ATM) switching network components as a translation table. Since ATM networks are connection-oriented, virtual circuits need to be set up across them prior to any data transfer. There are two kinds of ATM virtual circuits: Virtual Path (identified by a virtual path identifier or VPI) and Channel Path (identified by a channel path identifier or VCI). VCI/VPI values are localized; each segment of the total connection has unique VPI/VCI combinations. Whenever an ATM cell travels through a switch, its VPI/VCI value has to be changed into the value used for the next segment of connection. This process is called VPI/VCI translation. Since speed is an important factor in ATM network, the speed at which this translation occurs forms a critical part of the network's overall performance.

CAM can act as an address translator in an ATM switch and perform the VPI/VCI translation very quickly. During the translation process, the CAM takes incoming VPI/VCI values in ATM cell headers and generates addresses that access data in an external RAM (since standard CAM architectures cannot support the required capacity, a CAM/RAM combination enables the realization of multi- megabit translation tables with fully-parallel search capability). VPI/VCI fields from the ATM cell header are compared against a list of current connections stored in the CAM array. As a result of the comparison, CAM generates an address that is used to access an external RAM where VPI/VCI mapping data and other connection information is stored. The ATM controller modifies the cell header using the VPI/VCI data from the RAM and the cell is sent to the switch[5].

ATM CONTROLLER

The basic functionality of the controller is to receive ATM cells from the PHY via the utopia interface, utilize the cell header to determine what channel related to this FCC the cell belongs to, and transfer the data from the cell to the next available location in the appropriate buffer. The reverse is also true. When the PHY indicates that it has room for a cell to transmit the controller must decide which is the next channel to be transmitted, locate the buffer containing the required cell, add the appropriate header to the cell, and transfer the cell to the PHY.

This is a very simple description of the activity and as you progress through the course the process will be described in more detail. The process of segmentation and re-assembly is simply the transfer of the required data between the cells and buffers, where the cell contains the fixed block of data between 46 and 48 bytes depending on the adaptation layer used, and the buffers contain the user data of whatever size it is. Address Mapping is the Address header and appropriate channel. Buffer is the way of another protocol. ATM Many Channel all the information handled by the connection table. Below the Fig 3.1 to overall explanation for the separate blocks[6].

A. Memory Structure

For the ATM function to operate parameters are required for each channel.

There are address compression tables for the receiver to decide which channel any given cell relates to, connecti1on tables for both receiver and transmitter for defining all the protocol and data routing information for each channel, pace control tables for directing the scheduling of cell to transmit, Interrupt queues for both receive and transmit, and buffer descriptors and buffers for the data.

Some of these parameters are in DP RAM ,some in external memory.

FCC buffering is an intermediate buffer to improve data throughput and where some processing is handled by the CP and the register area is where the basic functionality of the FCC is defined.

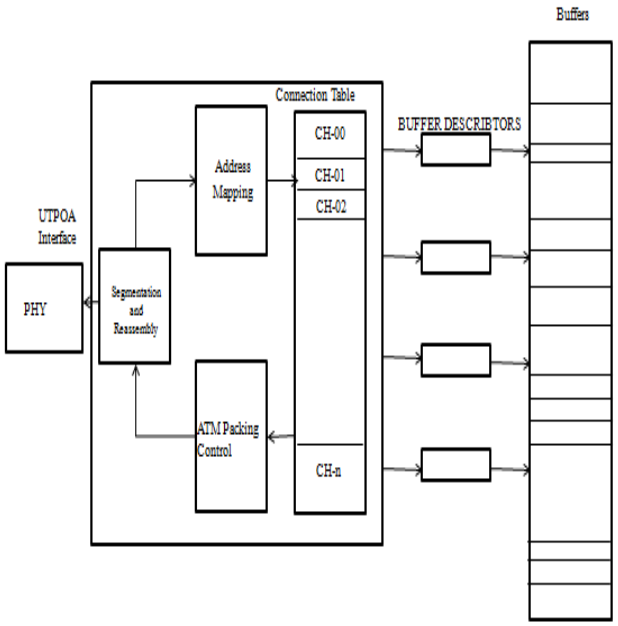


Figure 3: ATM Controller

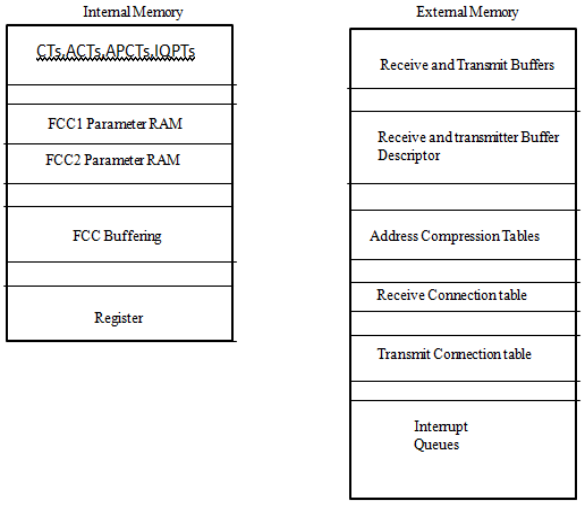


Figure 4: Memory Structure

B. VPI/VCI Evaluation

VPI is the virtual path identifier and can be considered like the outer case of a multi core cable. It identifies the major route of the data. VCI is the virtual circuit identifier and can be considered like an inner core of the cable.

These values are used to route the cell data to the required destination. However, the difficult concept here is that when the cell is transmitted, these values are not defining the final destination but simply the first stage routing.

A very brief explanation of what happens is that before any data is transmitted the system has to through a form of negotiation to find the best routing for the cell and in the process each node or ATM switch must set up a table for the VPI and VCI values, and priority and quality of service for the transfer.

This is all handled by higher level applications software outside the FCC operation and so is not a function of this training. The VPI and VCI is added into the header of the cell when transmitted, and the receiver examines these values to determine which channel the cell belongs to.

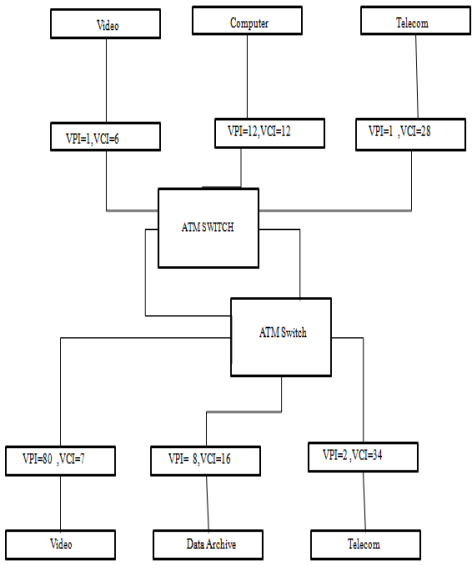


Figure 5: ATM Network VPI/VCI

SIMULATION RESULT ANALYSIS

The proper Operation of both power optimized and Speed Optimized designs are verified by performing extensive Microwind and Dsch &Xilinx simulation. All simulation presented this section compare ML0 against an ML1 on 144 bit CAM Word.

A. Design Optimized for Power Consumption

For accurate Comparison of the ML voltages, the initial currents to all the ML Must be identical. For minimum Power Consumption initial current must be zero.and the pre charging node Vdd-Vtn.

Table 4.1 and Table 4.2 shows the Xilinx Simulation results for this design compares the power level for 144 bit CAM Word.

Table 1: Existing Method Power Analytical

Power Summary	I(mA)	P(mW)
Total power Estimated Power Consumption	0	118
Vccint l00v	62	111
Vcce Quicien	2	7
Clocks	38	69
Input	8	15
Logic	0	0
Output	-	-
Signals	0	0
Quicient Vccint l00v	15	27
Quicien Vcc33. 3,0	2	7

Table 2: Existing Thermal Summary

Estimated Junction Temperature	27*c
Ambient Temperature	25*c
Case Temperature	27*c
Theta J-A	17c/W

Comparison table power consumption vs Thermal power. Two types of Analytical progress various types of Parameter should be Analyzed. In this Existing method Estimate Power Consumption 118 P(mW) at the same time Temperature level 27*C. Clock pulse 69 clock P(mW).

In this Existing Method Concepts fully pre Computation Based CAM. Is also Used Parity CAM in the proposed system. Various Technology is Used to find the Efficient Power Consumption.

Table 3: Proposed Method Power Analytical

Power Summary	I(mA)	P(mW)
Total power Estimated Power Consumption	0	115
Vccint l00v	60	109
Vcce Quicien	2	7
Clocks	37	67
Input	8	15
Logic	0	0
Output	-	-
Signals	0	0
Quicient Vccint l00v	15	27
Quicien Vcc33.3,0	2	7

Table 4: Proposed Method Thermal Summary

Ambient Temperature	25*c
Case Temperature	27*c
Theta J-A	17c/W

B. Design Optimized for Search speed

To increase Search Speed ,the initial Current supplied MLs is increased by Pre Charging the VAR node.

Speed Grade: -7

Table 5: Existing Search Speed

Minimum period:	3.680ns (Maximum Frequency: 271.739MHz)
Minimum input arrival time before clock	5.892ns
Maximum output required time after clock	8.129ns
Maximum combinational path delay	No path found

Proposed system Search speed

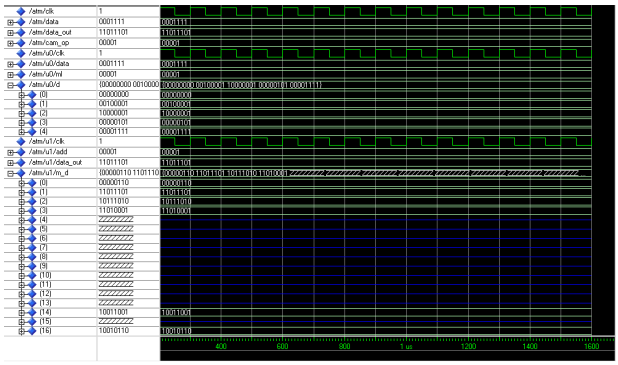
Speed Grade: -7

Table 6: Proposed Search Speed

Minimum period	1.714ns (Maximum Frequency: 583.431MHz)
Minimum input arrival time before clock	4.476ns
Maximum output required time after clock	8.129ns
Maximum combinational path delay	No path found

To Compare Existing and Proposed System Clock Speed Differents of the Maximum input arrival rate 1.416 nsec. But maximum Output required time after clock is same.

CALCULATING RESULT ANALYSIS SPEED VS POWER CONSUMPTION



CONCLUSION

The Proposed CAM allocates power to match decision based on the number of mismatchd bits in each CAM Word. This scheme result considerable power reduction. The Proposed System Power Consumption 115 P(mW).Existing Method Power Consumption 118 P(mW). Then the input arrival rate both are the Difference is 1.416nsec.Power consumption Avg 0.9754% Variations and then avg speed is 1.416nsec.

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