ISSN 2348-375X

Unique Journal of Engineering and Advanced Sciences

Available online: www.ujconline.net

Research Article

IMPLEMENTATION OF HIGH EFFICIENT DSVPWM TECHNIQUE BASED INVERTER FOR THREE PHASE MOTOR

Jeny Francina A[1*], Sharmilee K[2], Marimuthu CN[3]

[1]PG Scholar, Nandha Engineering College/ECE, Tamilnadu, India
[2]Associate Professor, Nandha Engineering College/ECE, Tamilnadu, India
[3]Prof & Dean, Nandha Engineering College/ECE, Tamilnadu, India

Received: 11-12-2013; Revised: 10-01-2014; Accepted: 08-02-2014

*Corresponding Author: **Jeny Francina A**, Email: jenyfrancina@gmail.com

ABSTRACT

This paper presents an Implementation of High Efficient DSVPWM Technique Based Inverter For Three Phase Motor with field programmable gate array (FPGA)-based control integrated circuits (IC) used in power conditioning system for ac-voltage regulation. Digital Space vector pulse width modulation (DSVPWM) algorithm provides maximum flexibility to optimize switching waveform. In this system, double edge triggering was implemented. It consumes less power compare to other conventional PWM techniques. The DSVPWM pulses thus generated through Xilinx is given as switching pulses to voltage source inverter(VSI) circuit to trigger the three phase motor. The delay time of PWM output is programmable and DSVPWM control IC is reprogrammable. It shows the advantage of lower total harmonic distortion (THD) without increasing the switching losses. Here results are provided along with simulation analysis in terms of THD, output fundamental voltage and voltage transfer ratio to verify the feasibility of operation. The DSVPWM switching pattern has been achieved with a fundamental frequency of 50HZ.

Keywords: DSVPWM, Double edge triggering, FPGA, THD, Xilinx, switching losses

INTRODUCTION

In various emerging power electronic devices, switching power converters are used in solid state power devices and microprocessors to convert and deliver the required energy to the motor drives. Mostly in Industrial applications, variable frequency ac drives are used. Pulse width modulated (PWM) dc-ac converters have a wide range of applications in ac motor drives and ac power conditioning systems[1]. The PWM strategy plays an important role in the minimization of harmonics and switching losses in these converters, especially in the three-phase applications. Various modulation strategies, control schemes, and realization techniques[2].

The important factors needed to be considered in the IC design of PWM control are simplicity, flexibility and complexity. According to the modulating signal, width of the pulses changes from each other. So, that these PWM pulse signal can be applied to the gate of a power transistor where it causes the transistor to turn on and turn off at each and every intervals of various PWM signals. As the modulation is concerned the space vector modulation (SVM) has attracted great interest in recent years. Because harmonic losses are minimum compared to other methods. The main advantage is that lower THD without increasing the switching losses. But because of the computational complexity of those techniques Digital SVPWM design technique is presented. These new type of converters are suitable for high voltage and high power application due to their ability to synthesize waveforms with better harmonic spectrum.

Thus this paper demonstrates that a more efficient and faster solution is the use of Field Programmable Gate Array (FPGA's), it investigates how to generate a variable PWM waveform based on Xilinx FPGA and the proposed design is tested by functional/timing simulation and experiments. The rest of the paper is organized as follows. Section II Graphical representation of a three phase inverter circuit. Section III briefly introduces the basic principle of symmetrical space vector PWM method. Section IV details on FPGA implementation process. Section V the block diagram representation of the hardware . Section VI explains the experimental results. and Section VII is the conclusion.

VARIOUS THREE PHASE INVERTER CIRCUITS

The cascaded multilevel inverter is one of the most familiar topologies in the Industrial applications. It has been used because of its massive features such as simple circuitry, minimum number of components structure modular and unbalance capacitor voltage problem avoidance. Though it has so many advantages because of its increased number of output voltages the circuit becomes huge due to increase in number

of power devices. In this project, it is proposed to employ a new technique to obtain a multilevel output using less number of power semiconductor switches when compared to ordinary cascaded multilevel inverter[3].

The inverter consists of seven MOSFET switches and three separate DC sources with a load. By switching the MOSFETS at the appropriate firing angles, we can obtain the seven level output voltage. MOSFET is preferred because of its fast

Switching nature. Recent development in high switching frequency power devices are such as IGBT, offers the possibility of developing high frequency PWM control techniques.

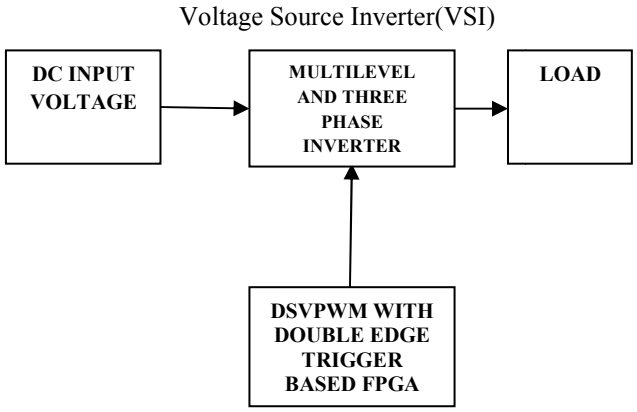

Figure 1: Block diagram of proposed FPGA based DSVPWM control

PRINCIPLE OF SPACE VECTOR PWM

Principle of Pulse Width Modulation (PWM)

Fig. 2 shows circuit model of a single-phase inverter with a center-taped grounded DC bus,and Fig 3 illustrates principle of pulse width modulation.

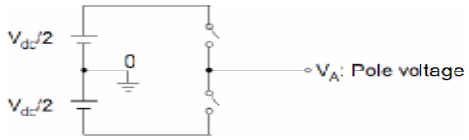

Figure 2: Circuit model of a single-phase inverter.

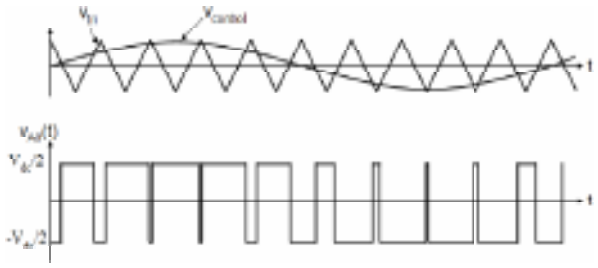

Figure 3: Pulse width modulation.

As depicted in Fig. 3, the inverter output voltage is determined in the following:

- When Vcontrol > Vtri, VA0 = Vdc/2
- When Vcontrol < Vtri, VA0 = −Vdc/2

Also, the inverter output voltage has the following features:

- PWM frequency is the same as the frequency of Vtri
- Amplitude is controlled by the peak value of Vcontrol
- Fundamental frequency is controlled by the frequency of Voltage (V) control

Basic Principle of Space Vector PWM

The circuit model of a typical three-phase voltage source PWM inverter is shown in Fig. 4.

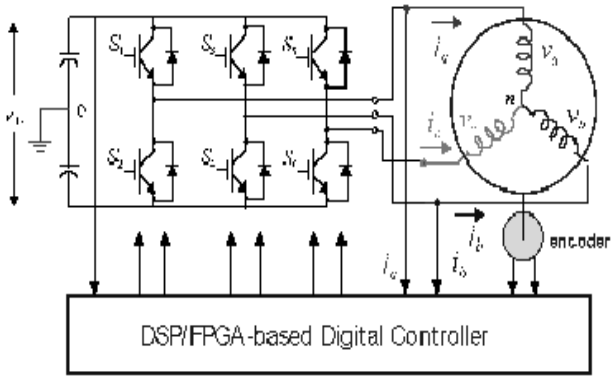

Figure 4: Circuit schematics of a voltage-source full-bridge three-phase PWM inverter.

In the above Fig.4 S1 to S6 are the six power switches that shape the output, which are controlled by the switching variables a, a′, b, b′, c and c′. When an upper transistor is switched on, i.e., when a, b or c is 1,The corresponding lower transistor is switched off, i.e., the corresponding a′, b′ or c′ is 0.Therefore, The on and off states of the upper transistors S1, S3 and S5 can be used to determine the output voltage.

The relationship between the switching variable vector [a, b, c]t and the line-to-line voltage

$$\begin{bmatrix} V_{ab} \\ V_{bc} \\ V_{ca} \end{bmatrix} = V_{dc} \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix} \begin{bmatrix} a \\ b \\ c \end{bmatrix}$$

[4] vector [Vab Vbc Vca]t is given by in the following:

$$\begin{bmatrix} V_{an} \\ V_{bn} \\ V_{cn} \end{bmatrix} = \frac{V_{dc}}{3} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \begin{bmatrix} a \\ b \\ c \end{bmatrix}.$$

As illustrated in Fig. 4, there are eight possible combinations of on and off patterns for the three upper power switches. The on and off states of the lower power devices are opposite to the upper one and so are easily determined once the states of the upper power transistors are determined. the eight switching vectors, output line to neutral voltage (phase voltage), and output line-to-line voltages in terms of DC-link Vdc, are given in Table1 and Fig. 5 shows the eight inverter voltage vectors (V0 to V7).

Table 1: Voltage Vectors, Switching vectors, phase voltages and t line to line voltages

Voltage Vectors	Switching Vectors			Line to neutral voltage			Line to line voltage		
	a	b	c	V_{an}	V_{bn}	V_{cn}	V_{ab}	V_{bc}	V_{ca}
V_0	0	0	0	0	0	0	0	0	0
V_1	1	0	0	2/3	-1/3	-1/3	1	0	-1
V_2	1	1	0	1/3	1/3	-2/3	0	1	-1
V_3	0	1	0	-1/3	2/3	-1/3	-1	1	0
V_4	0	1	1	-2/3	1/3	1/3	-1	0	1
V_5	0	0	1	-1/3	-1/3	2/3	0	-1	1
V_6	1	0	1	1/3	-2/3	1/3	1	-1	0
V_7	1	1	1	0	0	0	0	0	0

Figure 5: The eight inverter voltage vectors (V0 to V7).

Digital Space Vector PWM (DSVPWM) refers to a special switching sequence of the upper three power transistors of a three-phase power inverter. It has been shown to generate less harmonic distortion in the output voltages and or currents applied to the phases of an AC motor and to provide more efficient use of supply voltage compared with sinusoidal modulation technique as shown in Fig. 6.

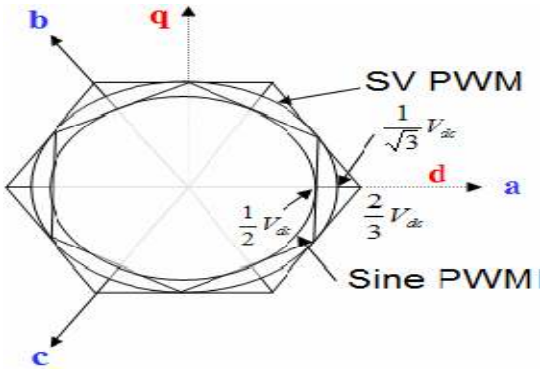

Figure 6: Locus comparison of maximum linear control voltage in Sine PWM and DSVPWM.

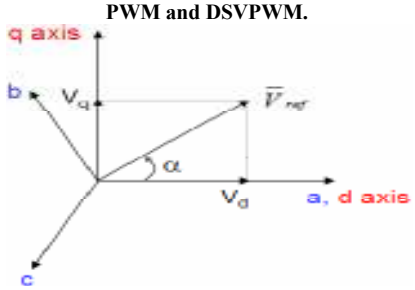

Figure 7: The relationship of abc reference frame and stationary dq reference frame

$$\mathbf{f}dq0 = \mathbf{K}s\mathbf{f}abc$$

As described in Fig. 7, this transformation is equivalent to an orthogonal projection of [a, b,c]t onto the two-dimensional perpendicular to the vector [1, 1, 1]t (the equivalent d-q plane) in a three-dimensional coordinate system. As a result, six non-zero vectors and two zero vectors are possible. Six nonzero vectors (V1 - V6) shape the axes of a hexagonal as depicted in Fig. 8, and feed electric power to the load. The angle between any adjacent two non-zero vectors is 60 degrees. Meanwhile, two zero vectors (V0 and V7) are at the origin and apply zero voltage to the load. The eight vectors are called the basic space vectors and are denoted by V0, V1, V2, V3, V4,V5, V6, and V7. The same transformation can be applied to the desired output voltage to get the desired reference voltage vector Vref in the d-q plane.The objective of space vector PWM technique is to approximate the reference voltage vector Vref using the eight switching patterns. One simple method of approximation is to generate the
average output of the inverter in a small period, T to be the same as that of Vref in the same period.

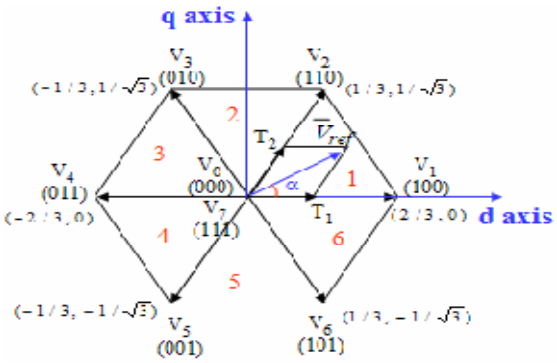

Figure 8: Basic switching vectors and sectors

Therefore, space vector PWM can be implemented by the following steps:

Step 1. Determine Vd, Vq, Vref, and angle (α)

Step 2. Determine time duration T1, T2, T0

Step 3. Determine the switching time of each transistor (S1 to S6)

Step 1: Determine Vd, Vq, Vref, and angle (α)

From Fig. 7, the Vd, Vq, Vref, and angle (α) can be determined as follows.

Step 2: Determine time duration T1, T2, T0

From Fig. 10, the switching time duration can be calculated as follows:

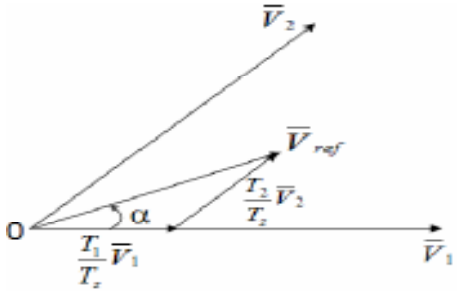

Figure 10: Reference vector as a combination of adjacent vectors at sector 1.

Step 3: Determine the switching time of each transistor (S1 to S6)

Simulation Steps:

(1) Initialize system parameters in MATLAB/SIMULNK.

(2) Perform M-File coding to

i. Determine sector

ii. Determine time duration T1, T2, T0

iii. Determine the switching time (Ta, Tb, and Tc) of each transistor (S1 to S6).

iv. Generate the inverter output voltages (VAB, VBC, VCA,)

v. Generate VHDL Codings through software conversion tool

vi. Burn the program in the FPGA kit

(3) View the DSVPWM waveforms through xilinx.

FIELD PROGRAMMABLE GATE ARRAY

A Field-Programmable Gate Array or FPGA is a silicon chip containing an array of configurable logic blocks (CLBs). Unlike an Application Specific Integrated Circuit (ASIC) which can perform a single specific function for the lifetime of the chip an FPGA can be reprogrammed to perform different function in a matter of microseconds. The design used Xilinx development tools, namely Workview, and is realized in a single FPGA chip with no external memory[5]. The benefits of this design are as follows

- The whole system is implemented in only a single chip consequently the circuit is very compact.
- Systems of FPGA chip are more reliable because they do not need any control software
- Faster design and verification time, design change without penalty.

In this paper programming FPGA using Hardware Description Languages and coding are used to generate the Space Vector Modulation for the inverter circuit. The point to be noted here is that instead of writing the direct VHDL Codings firstly the M-File codings are written to generate the DSVPWM pulses and then after by using the software converter VHDL coding are generated.Therby the work requires less time and fast operation[9].

The MATLAB/SIMULNK environment is familiar to vast number of software programmers and since m-file coding is very much common to most of the programmers it becomes easier for individuals to work in this software.

A very attractive high-level design/simulation tool is provided by FPGA and is called XILINX. It is a very flexible design tool, which allows Testing of a high-level structural description of the design and makes possible quick changes and corrections. The circuit description structure is very similar to the way the design could be implemented later. Therefore mapping tool allowing conversion of such a structure into VHDL code would save the designer's time, which otherwise has to be spent in rewriting the same structure in VHDL and probably making mistakes that will need debugging.

HARD WARE OF GENERAL BLOCK DIAGRAM

As per the above block diagram the hardware components are arranged in a précised manner to design the high performance efficient inverter for a three phase motor used in industrial applications. The input signal was given to the sin/cos generator and also vector DQ axis duty generator. The output of generators are given as the input for the 2/3 co ordinator converter and phase duty calculator which calculates the phase cycles used to operate the DSVPWM generator. DSVPWM block produces the trigger pulses which is to drive the induction motor. The opto coupler is used in between the DSVPWM generator and driver to isolate the digital and high voltage analog circuits. The driver circuit offered the high voltage which is required by the inverter. Finally the voltage inverter is connected to the induction motor the industrial load.

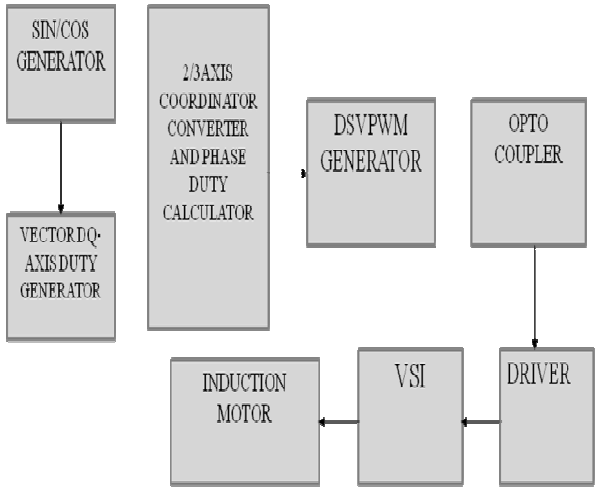

Figure 11: Block diagram representation of Hardware implementation

EXPERIMENTAL RESULTS

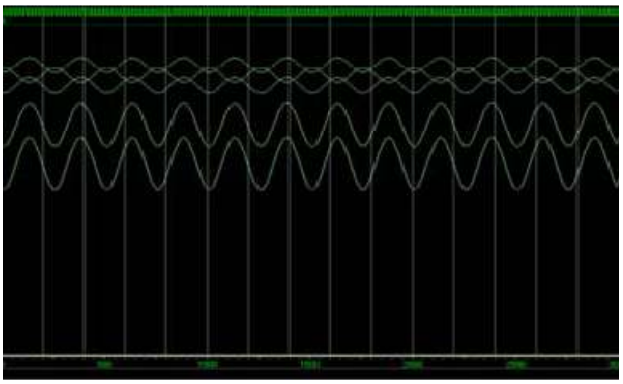

Figure 12: Three to Two axis converter. (Va, Vb, Vc) are transformed into (Vα, Vβ)

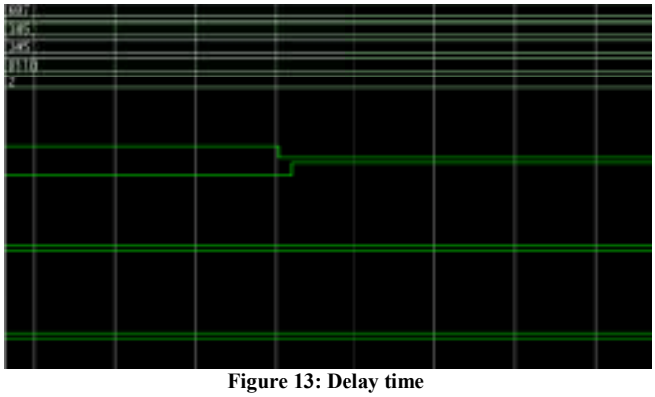

Figure 13: Delay time

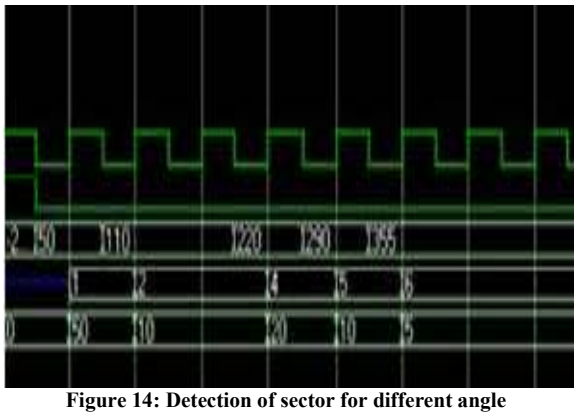

Figure 14: Detection of sector for different angle

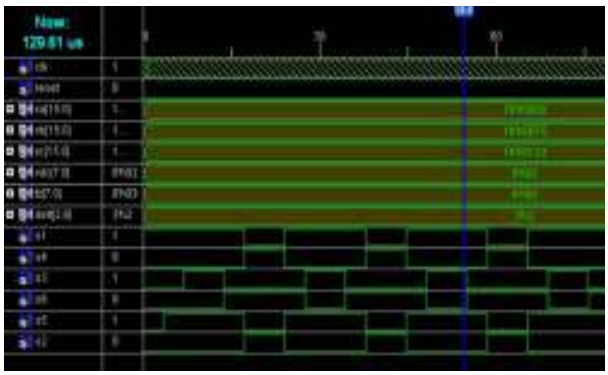

Figure 15: Output of each inverter

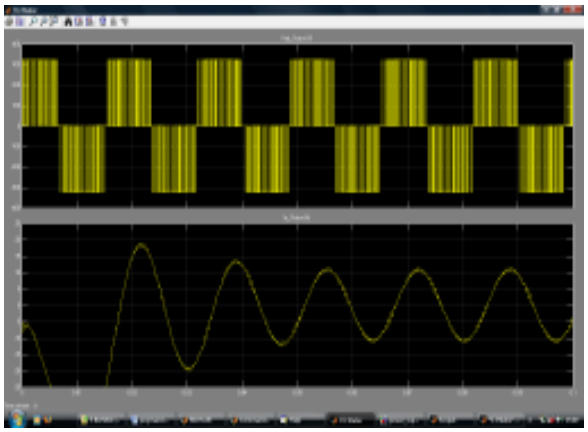

Figure 16: Response of stator voltage Vab and stator current Ia versus

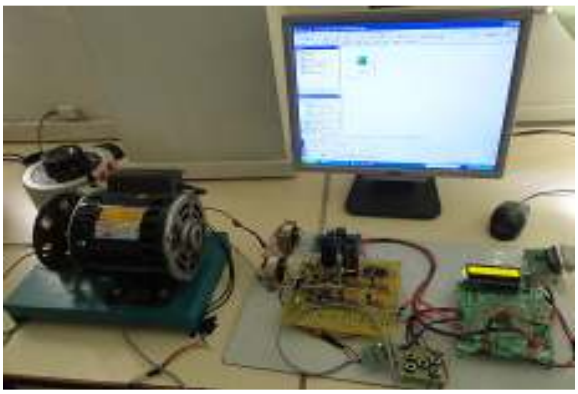

Figure 17: Hardware implementation of inverter design using FPGA

CONCLUSION

The FPGA is used to implement the DSVPWM control IC design. So, the overall design is controllable and reprogrammable. The fundamental frequency used for implementation is 50hz. And also it can be varied from 1.47Hz to 1.6kHz. The switching frequency of the PWM pulse output signal is 192Hz to 47.82kHz.The switching pattern generated by the inverter design will reduce the harmonic content in the final result. So, the system effectiveness and its reliability will be increased. This project deals with both theoretical and practical solution.

On the other hand since Field programmable gate array (FPGA) have better advantages compared to microprocessor and DSP control, this modulation technique is implemented in an FPGA by initially generating m-file through Matlab-Simulink environment. The FPGA coding makes it easier in designing the vector modulation pattern generator using field programmable Array .Although this project has more advantages it has some disadvantage that is it is difficult to perform when it is used with hysterisis based system.

REFERENCES

1. Vander Broek HW, Skudelny HC., and Stanke GV, Analysis and realization of a pulse width modulator based on voltage space vectors', IEEE Trans. Ind. Applicat., 2004; 24: 142–150.
2. Yu Z, Mohammed A, and Panahi, A review of three PWM techniques, in Proc. Amer. Control Conf., 1997; 256– 261.
3. Chung DW, Sul SK, Unified voltage modulation technique for real-time three- phase power conversion, IEEE Trans. Ind. Appl., 2000; 34 (2):.374-380.
4. Devarajan Prawin N Angel Michael, Design and implementation of FPGA Based Induction Motor Drive, IJRTET, ACEEE, 2010; 3: 3.
5. Franquelo L, Three-dimensional spacevector modulation algorithm for four-leg multilevel converters using abc coordinates', IEEE Trans. Ind. Electron., 2006; 53 (2): 459-466.
6. Jin-Woo Jung, Ph.d Student, Ohio State University. Space Vector PWM Inverter.1998.
7. Klima J, Analytical model for the time and frequency domain analysis of space- vector PWM inverter fed induction motor based on the Laplace transform of space-vectors', in Proc. Power Conversion Conf., Osaka, Japan, 2002; 1334 –1339.
8. Martin JP, Semail E , Pierfederici S, Bouscayrol A, and B. Davat, Space vector control of 5-phase PMSM supplied by 5 H-bridge VSIs'in Proc. Congr. Int. Electrimacs 2002.
9. Reddy BV, Somasekhar VT, and Kalyan Y, Decoupled space-vector PWM strategies for a four-level asymmetrical open-end winding induction motor drive with waveform symmetries', IEEE Trans. Ind. Electron, 2011.

Source of support: Nil, Conflict of interest: None Declared