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Research Article

DESIGN OF AREA EFFICIENT FIR FILTER USING TRUNCATED MULTIPLIER TECHNIQUE FOR DSP APPLICATIONS

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ABSTRACT

Multiplication of two numbers is one of the most area consuming arithmetic operations in high-performance circuits as it generates a product with twice the original bit width. The truncation of product bits to the required precision of truncated multipliers offers significant improvements in area, delay and power. The proposed method reduces the number of full adders and half adders during the tree reduction. Usually the product of two numbers appears as output in the form of LSB and MSB. The LSB part is truncated and compressed using MCMAT technique. In previous related papers, the truncation error is reduced using MCMT technique. In this project, truncation error is not more than 1 ulp (unit of least position). While implementing the proposed method experimentally, there is no need of any error compensation circuits and the final output is precised. Hence the area can be saved and the power is also reduced. To further extend the work, digital FIR filter implementation with MCMAT technique is carried out using Wallace Tree Compressor (WTC).

Keywords: Multiplication, Truncated multipliers, MCMT, MCMAT, WTC.

INTRODUCTION

Multiplication is frequently required in digital signal processing for filter realization. Many research works deals with the low power design of high speed multipliers. Normally, multiplication involves two basic operations as partial production generation and their partial product summation, performed using two kinds of multiplication algorithms, serial and parallel. Serial multiplication algorithms use sequential circuits with feedback: inner products are sequentially produced and computed. Parallel multiplication algorithms often use combinational circuits and do not contain feedback structures. Multiplication of two bits produces an output which is twice that of the original bit. It is usually to truncate the partial product bits to the required precision to reduce the area cost[1-5].

In the project, digital FIR filter is designed with Multiple Constant Multiplication Accumulation Truncation (MCMAT) technique using WTC which reduces the number of full adders and half adders during the tree reduction using carry propagation addition. The design achieves less area and power which leads to have truncation error of not more than 1 ulp (unit of least position). So there is no need of error compensation circuits hence the final output will be precised. Since the multiplication of two numbers is one of the most area consuming arithmetic operations in high-performance circuits as it generates a product with twice the original bit width. The truncation of product bits to the required precision of truncated multipliers offers significant improvements in area, delay and power. This design is analyzed in terms of area and power with respect to the nominal implementation of the multiplier in FIR filter[6-10].

This paper is organized as follows. In Section II, discusses the PP truncation and compression schemes. In Section III, describes the truncated multiplier technique using Wallace tree compressor. In Section IV, the proposed scheme is implemented in FIR filter realization. In Section V, the proposed scheme is compared to the previously proposed ones. Finally, Section VI, concludes this paper.

II. PP TRUNCATION AND COMPRESSION SCHEMES

A Truncated multiplier design usually consists of three stages, i.e., PP (Partial product) generation, PP reduction and final carry propagation addition (CPA). PPB (Partial product bits)

are generated from the multiplicand and multiplier. PP compression is to be taken place in the PP reduction. Finally the partial products bits are summed using carry propagate addition.

1. MCMT
2. MCMAT

A. Scheme 1

Multiple Constant Multiplication Truncation (MCMT) module performs the concurrent multiplications of individual delayed signals and respective filter coefficients. Here truncation of product bits is performed for each partial product generation. More numbers of adders are required for each partial product summation since no accumulation of product bits are carried out. As more columns are eliminated compared to the standard multiplier, the area and power consumption of the arithmetic unit are significantly reduced, and in many cases the delay also decreases.

B. Scheme 2

Multiple constant Multiplication Accumulation Truncation (MCMAT) technique is more efficient to collect all the Partial Product (PPs) into a single Partial Product Bit (PPB) matrix with Carry Propagation Addition (CPA). It is needed to truncate the partial product bits to the required precision to reduce area cost. In this technique, a single row of PPBs is made undeletable (for the subsequent rounding), and the PPB elimination consists of only deletion and rounding.

Instead of accumulating individual multiplication for each product, it is more efficient to collect all the PPs into a single PPB matrix to reduce the height of the matrix to two, followed by final carry propagation adder is shown in Fig.1. The MCMAT truncated multiplier consists of several operations, including deletion, reduction, truncation, rounding, and final addition.

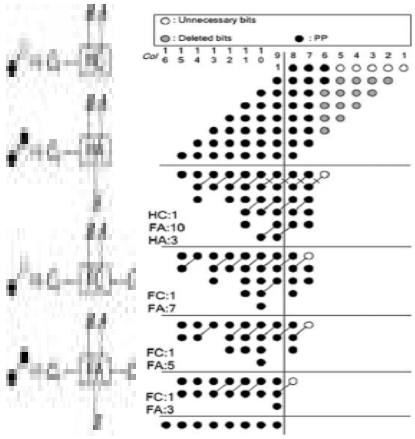

Figure 1:Truncated multiplier design using MCMAT technique

In the first step, we perform the deletion that removes all the unnecessary PP bits that do not need to be generated is shown in Fig.1. The deletion of PP bits starts from column 3 by skipping the first two rows of PP bits because after applying reduction, the resultant two rows will be removed in the subsequent truncation and rounding processes. After the deletion of PP bits, we perform the per-column reduction and generate two rows of PP bits. After reduction, we perform the truncation that further removes the first row of n − 1 bits from column 1 to column n− 1.This step of truncation introduces truncation error[11-13].

After deletion, reduction, and truncation, the PP bits are added using a CPA to generate the final product of P bits. The bits in column 2 to column n−1can be safely removed before CPA because these bits are the only bits left in the columns after the deletion and truncation processes, and thus, they do not affect the carry bit to column n + 1 during the rounding process. Before the final CPA, we add a bias constant of 1/2 ulp in order to achieve the round to nearest rounding with the rounding error. The bit at column n after the final CPA is also removed during the rounding process.

Thus, the total error for the design of the MCMAT multiplier is bounded by

$$-ulp < E = (E_D+E_T+E_R) \leq ulp$$

III. PROPOSED TRUNCATED MULTIPLIER TECHNIQUE USING WALLACE TREE COMPRESSOR

A Wallace Tree Compressor (WTC) is a technique that is used to increase the speed of the partial product addition operation with MCMAT. The Wallace Tree Compressor (WTC) can be 4:2, 5:2, 6:2 or 7:2. The 5:2 wallace tree compressor has 5 inputs and produces 2 outputs is shown in Fig.2. The 5:2 WTC can be implemented using full adder and half adder. In the first stage, i1,i2,i3 are given as input to full adder and s1, c1 are obtained as output. In the second stage, cin1(i5) and i4 are given as input to the half adder and s2 and c2 are obtained as output. In the third stage, s1 and s2 additions are performed using half adder and final sum, c3 are obtained as output. In the final stage of 5:2 WTC, c1, c2 and c3 are given as an input to the full adder and final carry and cout are obtained as output. As a final result, sum, carry and cout are obtained from the Wallace Tree compressor (WTC)[14].

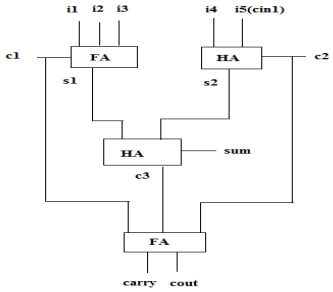

Figure 2: Wallace Tree Compressor (5:2).

IV. PROPOSED WORK IN FIR FILTER REALIZATION

Truncated multiplier can be effectively implemented in FIR filter structure[8]. Conventional FIR filter performs ordinary multiplication of coefficient and input without considering the partial product bit length. Thus the structure can be made effective by replacing the existing multiplier with the proposed MCMAT truncated multiplier technique using Wallace Tree Compressor for visible area reduction. Digital FIR filter implementation using MCMAT technique that removes unnecessary PPBs so that truncation error is not more than 1ulp.

In Fig. 3., the white circles in the L-shape block represent the undeletable PPBs. The deletion of the PPBs is represented by

gray circles. After PP compression, the rounding of the resultant bits is denoted by crossed circles. The last row of the PPB matrix represents all the offset and bias constants required including the sign bit modifications. The proposed work of digital FIR filter design is implemented with MCMAT technique using Wallace tree compressor(5:2), where the results of the FIR filter structure shows the better area and power reduction compared to the conventional FIR filter[1].

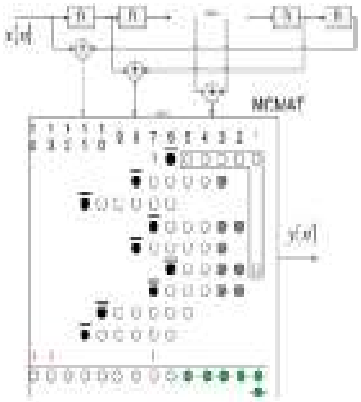

Figure 3: Digital FIR filter implementation using MCMAT technique

This modified FIR filter design and implementation can be divided into the following stages: Finding filter order and coefficients, coefficient quantization, digital FIR filter implementation with MCMAT technique using Wallace tree compressor is shown in Fig.4. In the first stage, the filter order and the corresponding coefficients are determined to satisfy the specification of the frequency response. Then, the coefficients are quantized to finite bit accuracy of 8 bits. The first two stages are implemented using MATLAB. Finally, optimization approaches such as MCMAT technique using WTC are used to minimize the area of hardware implementation[1].

An important issue of FIR filter implementation is the optimization of the bit widths for filter coefficients which has a direct impact on the area cost of adders, arithmetic units and registers. To overcome this problem, the proposed method is designed and implemented.

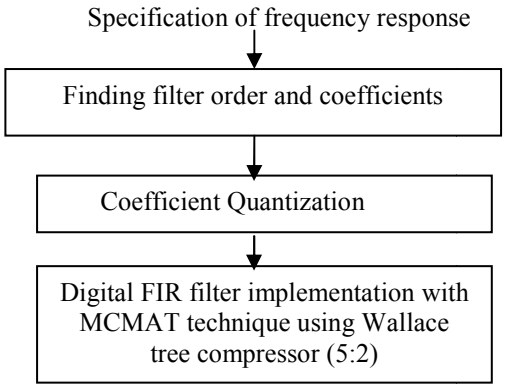

Figure 4: Digital FIR implementation with MCMAT technique using WTC.

V. EXPERIMENTAL RESULTS AND COMPARISONS

We implemented FIR filters with the low pass filter specification as given in Table I[15,16]. M is the original filter order while EWL is the effective word length, f_{pass} and f_{stop} are the passband and stopband edge frequencies normalized to one, and A_{pass} and A_{stop} denote the corresponding peak to peak ripples. Table II shows the implementation results for Filter A with 5 tap LP using Xilinx ISE simulator.

Table I: Specification of the FIR filter under consideration

Filter	M	EWL	f_{pass}	f_{stop}	A_{pass} (dB)	A_{stop} (dB)
A(LP)	5	8	0.15	0.25	0.09	46

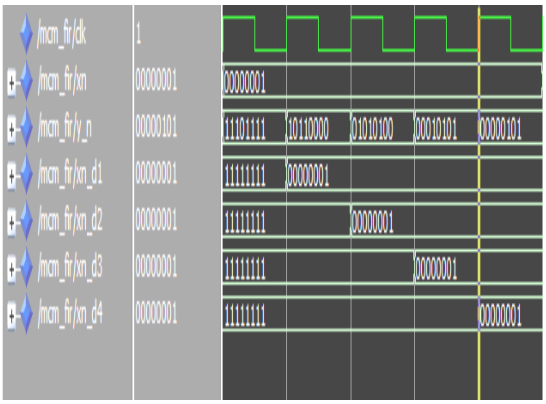

Figure 5: Simulation result of digital FIR implementation using MCMAT technique.

For the given specifications, digital FIR filter implementation using MCMAT technique is simulated using MODELSIM and the output is shown in Fig.5.Here xn is the input,d1,d2,d3,d4 are the filter coefficients and y_n is the output.

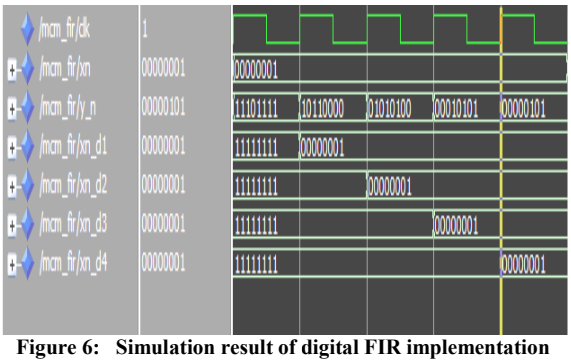

Figure 6: Simulation result of digital FIR implementation with MCMAT technique using WTC.

For the given specifications, digital FIR filter implementation with MCMAT technique using WTC (5:2) is simulated using MODELSIM and the output is shown in Fig.6.Here xn is the input, d1, d2, d3, d4 are the filter coefficients and y_n is the output.

From the synthesized result as given in Table II, it is found that the proposed truncated multiplier technique using WTC consumes low area and low power compared to existing truncated multiplier technique using MCMAT technique for FIR filter realization. Area utilization and power utilization by the proposed method is less.

Table II: **Synthesis results of Filter A with 5 tap LP**

Parameters	Digital FIR filter design using MCMAT technique	Digital FIR filter design with MCMAT technique using WTC
Area (gate counts)	2,363	2,136
Power (mw)	56.43	47.62
No. of latches	227	149
No. of Slice registers	246	169

After FIR filter operations, the output signals have larger bit width due to bit width expansion after multiplications. In many practical situations, only partial bits of the full-precision outputs are needed. For this purpose, design of area efficient FIR with MCMAT technique using WTC can effectively reduce the number of adders and the truncation error which is not more than 1 ulp ,and the final output will be précised.

VI. CONCLUSION

In this approach, digital FIR filter implementation with MCMAT technique using WTC produces truncation error which is not more than 1 ulp. So there is no need of error compensation circuits, and the final output will be précised. This design is analyzed in terms of area and power with the nominal implementation of the truncated multiplier. To verify the functionality of the multiplier, the MCMAT coded output values are obtained from modelsim.

The proposed digital FIR filter implementation with MCMAT technique using WTC is simulated using modelsim and the corresponding vcd files are generated. These vcd files are used to analyze the power and area of the digital FIR filter implementation using MCMAT technique. The area and power report of digital FIR implementation with MCMAT technique and MCMAT using WTC are obtained from Xilinx ISE compiler and it is found that nearly 10% of area is reduced and the reduction in power is about 16%.

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