ISSN 2348-375X

Unique Journal of Engineering and Advanced Sciences

Available online: www.ujconline.net

Research Article

EFFECTIVE DATA RETENTION AND NOISE SUPPRESSION IN MTCMOS CIRCUITS

Anoop G[1*], Angayarkanni N[2], Prasanna Venkitesan GKD[3]

[1]M.E VLSI Student, PGP College of Engineering and Technology, Nammakkal
[2]Assistant Professor. PGP College of Engineering and Technology, Nammakkal
[3]Vice Principal,HOD ECE Dept. PGP College of Engineering and Technology, Nammakkal

Received: 07-03-2014; Revised: 05-04-2014; Accepted: 03-05-2014

*Corresponding Author: **Anoop G,**
M.E VLSI Student, PGP College of Engineering and Technology, Nammakkal. E-mail: anoop.g774@gmail.com

ABSTRACT

Multi-threshold CMOS is commonly used for suppressing leakage currents in idle integrated circuits. Power and ground distribution network noise produced during SLEEP to ACTIVE mode transitions and data presevartion during sleep mode are important reliability concerns in MTCMOS circuits. Sleep signal slew rate modulation techniques for suppressing mode- ransition noise along with data retention technology is introduced in this paper. A triple-phase sleep signal slew rate modulation technique with a novel digital sleep signal generator with data retention mechanism utilising the same sleep signal is proposed. Reactivation time, mode-transition energy consumption, leakage power consumption, and layout area of different MTCMOS circuits are characterized under an equal-noise constraint. The proposed triple-phase sleep signal slew rate modulation technique enhances the tolerance to process parameter fluctuations by up to 183.1× as compared to various alternative MTCMOS noise suppression techniques in a UMC 80-nm CMOS technology.

Keywords: MTCMOS**,** Digital sleep signal slew rate modulator, low noise, mode transition energy, power and ground bouncing noise, process variations, reactivation time, sleep signal rise delay, triple-phase wake-up.

INTRODUCTION

MTCMOS is the most widely used leakage power reduction strategy in nanoscale integrated circuits when an idle circuit is awaken, significant voltage fluctuations occur on the power and ground distribution networks (power and ground bouncing noise). The active circuitry is disturbed due to the mode transition noise produced by an awakening circuit block. With more frequent and opportunistic mode transitions between the ACTIVE and SLEEP modes of operation, reactivation noise has become an important reliability concern in integrated circuit design. Data preserving during the sleep mode is an important concern while using the MTCMOS.A data retention technology is necessary and in this project an effective data retention technology with sleep signal as control signal.

Sleep signal slew rate modulation techniques are presented in this paper for ground bouncing noise suppression in MTCMOS circuits. Ground bouncing noise produced during SLEEP to ACTIVE mode transitions is an important reliability concern in multi-threshold CMOS (MTCMOS) circuits. Single-phase and multi-phase sleep signal slew rate modulation techniques are explored in this project to drastically suppress ground bouncing noise in MTCMOS circuits., leakage power consumption, and layout area of different MTCMOS circuits are characterized under an equi-noise constraint with a UMC CMOS technology.

Single-Phase Sleep Signal Slew Rate Modulation

Single-phase sleep signal slew rate modulation technique is presented in this section. The effect of sleep signal rise delay on ground bouncing noise produced by an MTCMOS circuit is evaluated. Circuits are designed with the UMC 80-nm multi-threshold voltage (multi- $_{Vth)}$ CMOS technology (high-Vth_nMOS = +370 mV, low-Vth_nMOS = +155 mV, high-Vth_pMOS = −310 mV, low-Vth_pMOS = −105 mV, and VDD = 1 V) . The ground bouncing noise phenomenon is evaluated with the parasitic impedance model of 40-pin dual in-line package. Post-layout simulation results are presented in the following sections to characterize different MTCMOS circuit techniques. The simulation temperature is 90 °C .

Sleep signal slew rate modulation techniques are evaluated with a ground-gated 33-bit Brent–Kung adder as illustrated in Figure 1. The sleep transistor is sized 5 µm to achieve

similar (within 5%) delay along the critical signal propagation path (in ACTIVE mode) of MTCMOS circuit as compared to the standard single low-| Vth| circuit.

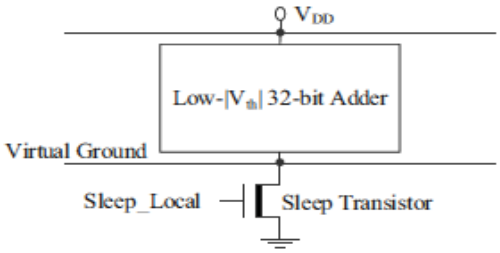

Figure 1: Ground-Gated 33-Bit Brent–Kung Adder

The rise delay is the time interval for the sleep signal to rise from 10 to 990 mV. when the rise delay of sleep signal is 60 ps (approximately the minimum achievable rise delay in this UMC 80-nm CMOS technology), the peak ground bouncing noise produced by the ground-gated 33-bit adder is 67.95 mV. Alternatively, when the rise delay of the sleep signal is extended by 1667 x to 100 ns, the peak ground bouncing noise is reduced by 148x down to 0.46 mV .

Multiple noise waveforms are generated as the sleep signal gradually rises from 0 V to $_{VDD}$ as. When the voltage level of sleep signal is lower than the threshold voltage (Vth_sleep) of sleep transistor, the sleep transistor operates in weak inversion region. The virtual ground line (VGND) is discharged very slowly by the small leakage current produced by the high-| Vth| sleep transistor. The noise induced on the ground distribution network is negligible for Vgs<Vth_sleep[1].

After the sleep signal rises above the threshold voltage of sleep transistor, the VGND is discharged faster. Noise on the real ground is thereby increased. Subsequently, when the VGND is discharged to one threshold voltage (low-Vth_nMOS) below the voltages of the internal nodes in the low-| Vth| circuit block, the parasitic capacitors of internal nodes start discharging as well. Another wave of bouncing noise is thereby produced on the real ground wires.

In SLEEP mode, VGND and all the internal nodes of low|Vth| circuit block are maintained at voltage levels close to VDD. During a reactivation event, the internal nodes of the low| Vth | circuit block transition to the correct logic states stage by stage depending on the primary input vectors. Some internal nodes follow the discharging VGND and transition toward 0 V. Significant amount of switching and short-circuit currents are produced by the awakening low-| Vth | logic block. Due to the high rate of change of the current produced by the sleep transistor (high di/dt), the ground bouncing noise is maximized. The switching and short-circuit currents through the low-| Vth | circuit block gradually disappear as the VGND voltage subsides and the internal node voltages stabilize. The noise on real ground is therefore gradually dampened. When the rise delay of sleep signal is relatively short (for example, 60 ps), all the switching and short-circuit currents are produced during a relatively narrow time frame. Alternatively, when the rise delay of sleep signal is increased, the switching and short-circuit currents are distributed to a longer time frame The rate of change of instantaneous currents is thereby reduced and the ground bouncing noise is mitigated., the peak ground bouncing noise produced by the ground-gated 33-bit adder is significantly reduced as the rise delay of sleep signal is increased from 60ps to 100 ns. The sleep signal slew rate modulation technique is effective in suppressing the ground bouncing noise produced by an MTCMOS circuit[1].

Stepwise Vgs MTCMOS

A stepwise Vgs MTCMOS circuit is activated in two steps as follows. In the figure 2, the sleep signal transitions from 0 V to an intermediate voltage level VX (0 V < VX < VDD) during the first step of a reactivation event. The sleep transistor is weakly activated with a low gate voltage (VX). Although the voltage swing on the VGND is relatively high during the first wake up step, the amplitude of the first noise waveform is suppressed due to the weak conductivity of the sleep transistor. After the VGND is discharged to a sufficiently low voltage level, the sleep signal transitions from VX to VDD. The sleep transistor is strongly turned on. VGND is discharged to 0 V following the full activation of the sleep transistor (Sleep Local=VDD). The amplitude of the second noise waveform is also suppressed due to the lower voltage swing on the VGND during the second wake up step.

A sleep signal modulator for stepwise Vgs MTCMOS circuit is presented in . During the first wake up step, N3 is turned on. Pdiv and N3 raise Sleep Local from 0 V to VX. The value of VX is determined by the voltage divider that is composed of the diode-connected pMOS transistor Pdiv, diode-connected nMOS transistor Ndiv, and N1. During the second wake up step, N3 is cut off, while Pcharge is activated. Sleep Local is raised from VX to VDD by Pcharge. While the stepwise Vgs is a potentially effective technique for mode transition noise suppression, many practical design challenges of stepwise Vgs MTCMOS circuits are over-looked in. The methodology needed to choose an appropriate intermediate voltage VX is not provided. The influence of sleep signal slew rate on reactivation noise is not discussed. The optimum VX that minimizes the peak reactivation noise varies with the threshold voltage of sleep transistor. The effectiveness of stepwise Vgs in suppressing reactivation noise is therefore strongly affected by process variations.

Triple Phase Slew Rate Modulation (Analog Circuit)

Slowly rising sleep signal is effective for suppressing the reactivation noise in MTCMOS circuits. A slowly rising sleep signal, however, also significantly increases the reactivation time and energy consumption of MTCMOS circuits[2]. The single-phase sleep signal slew rate modulation technique is therefore not suitable for fast and energy efficient power/ground gating in high-performance integrated circuits. An alternative triple-phase sleep signal slew rate modulation (TPS) technique is presented in to suppress the reactivation noise while accelerating the reactivation process in MTCMOS circuits., the sleep transistor produces negligible noise in the weak inversion region of operation (when Vgs<Vth_sleep). The sleep signal is preferred to rise faster from 0 V to the threshold voltage of sleep transistor in order to

reduce the overall reactivation time without producing significant noise. Reactivation noise is primarily produced after the sleep transistor is turned on. The sleep signal should be therefore subsequently decelerated as the gate voltage level reaches the threshold voltage of sleep transistor. Deceleration of sleep signal suppresses the peak mode transition noise that is produced after the sleep transistor is fully activated. After the VGND voltage is reduced to a very low level close to 0 V the mode transition noise diminishes to a negligibly low level. The rise of sleep signal should therefore be again accelerated to shorten the remaining duration of reactivation process. Due to the shorter periods of Phase_1 and Phase_3, the reactivation time and energy consumption of MTCMOS circuits are reduced.

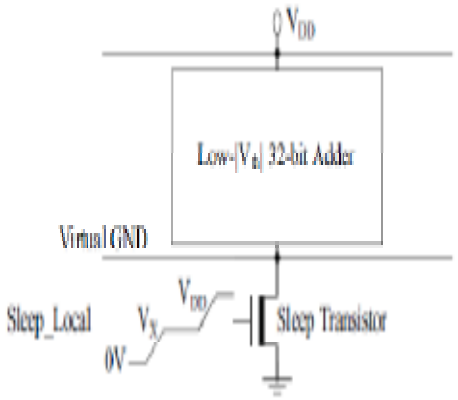

Figure 2: Stepwise vgs MTCMOS

The mixed-signal sleep signal modulator is shown in Fig. 3. The Vgs of sleep transistor is increased with small voltage steps. Additional clock signal and voltage bias sources (Vbias1, Vbias3, and Vbias3) are required for the operation of this mixed-signal circuit. Complex analog circuitry is employed to produce the three phases of sleep transistor activation. The mixed-signal sleep signal modulator consumes significant power and occupies a large layout area. The rising speed of sleep signal cannot be tuned individually during Phase_1 and Phase_3 with the sleep signal modulator that is described in . Phase_1 is inevitably elongated together with Phase_3to suppress the reactivation noise. The triple-phase reactivation time reduction that is achievable with this mixed-signal sleep signal generator is therefore limited. Furthermore, the sleep signal slew rates during Phase_1 and Phase_3 strongly depend on the value of C pump. Variations of C pump due to process fluctuations significantly degrade the effectiveness of this mixed-signal modulator for noise suppression.

Triple Phase Digital Sleep Signal Slew Rate Modulator

A new superior triple-phase fully digital sleep signal slew rate modulator is proposed in this section. The circuit is shown in Figure 4 Sleep Global is the input signal of the sleep signal modulator. Sleep Global triggers the activation and deactivation procedures of an MTCMOS circuit block. Sleep Local is produced by the proposed signal modulator and applied to the gate terminal of the footer that controls the ground connection of a local circuit block as shown in Figure 4. P1, P3, and P3 are used for tuning the slew rate of Sleep Local during the reactivation events that occur in three phases. In SLEEP mode, Sleep Global is "0". P1, P3, and P3are cut off. N discharge is turned on. Sleep Local is maintained at ~0V. The footer is cut off [3].

Sleep Global transitions from "0" to $_{VDD}$ to initiate a reactivation event. PH1 transitions low. P1 is turned on to start the first phase (Phase_1) of reactivation. Sleep Local starts to rise. When Sleep Local reaches the threshold voltage of Nsense_L (low-|Vth|), Nsense_L is turned on. EN1 (maintained at $_{VDD}$ in SLEEP mode) is discharged through Nreset1 and Nsense_L. PH1 transitions high. P1 is cut off. PH3 transitions low. P3 is thereby turned on to start the second phase (Phase_3) of reactivation where the sleep signal slew rate is reduced. The virtual ground line (VGND) is discharged primarily during Phase_3. Highest switching currents are produced in this phase as the internal nodes in the awakening low-|Vth| circuit block transition to the correct logic states. The rise of Sleep Local is intentionally decelerated by designing P3 to be significantly weaker as compared to P1. The peak ground bouncing noise produced by an awakening MTCMOS circuit is thereby mitigated[3].

When the virtual ground line is discharged to a sufficiently low voltage level, the voltage difference between Sleep Local and virtual ground line exceeds the threshold voltage of Nsense_H (high-|Vth|). Nsense_His turned on. EN3 (maintained at VDD in SLEEP mode) is discharged "Inverting_Delay_Chain", PH3 transitions low. P3 is turned on to start the third phase (Phase_3) of reactivation where the rate of change of Sleep Local is increased again. In Phase_3, weak P3 assists the significantly stronger P3 that is activated to raise Sleep Local faster towards VDD[4].With the triple-phase sleep signal modulator, the rising speed of sleep signal is adjusted by continuously monitoring the voltage level of Sleep Local. The transitions between the three phases of reactivation occur automatically. No additional control signal is required. So the complexity can be reduced, cost can be reduced. With the aggressive scaling of CMOS technology, the sub threshold leakage current is exponentially increased. One of the widely used leakage power reduction strategies is MTCMOS. In an MTCMOS circuit, high threshold voltage (high-) sleep transistors (header and footer) are used to cut off the power supply or the ground connection to the idle low threshold voltage circuit blocks to suppress the sub threshold leakage. When the MTCMOS technique is directly applied to a sequential circuit, such as a flip-flop (FF), the data in the storage element is lost during the sleep mode. A data-recovery process is typically necessary when the system is awakened from the sleep mode. The data recovery process during wake-up events causes significant degradation in system performance and increases the power consumption. The development of low-leakage sequential MTCMOS circuit techniques with low-cost and low-complexity data retention capability is therefore highly desirable. Several MTCMOS FFs that provide a low-leakage data preserving sleep mode are presented[4].

When a conventional sequential MTCMOS circuit transitions from the idle mode to the active mode, high instantaneous currents flow through the sleep transistors. Large voltage fluctuations occur on both the real power line (power bouncing noise) and the real ground distribution network (ground bouncing noise) . The employment of multiple autonomous power-gating domains is preferable for a more effective control of the leakage power consumption in MTCMOS integrated circuits.. Bouncing noise generated in one power-gating domain during a wake-up event is transferred through the shared power and ground distribution networks to the surrounding active circuit blocks. The node voltages and logic states of the active circuit blocks are thereby disturbed in a multi-domain MTCMOS circuit. The ground bouncing noise is expected to become an increasingly important reliability issue in future deeply scaled multi-domain MTCMOS integrated circuits with shrinking noise margins The SRAM -FF that is proposed in is a fusion of a static memory cell and an MTCMOS flip-flop with the standard ground-gating technique. An SRAM look- alike data retention cell is combined with the slave latch to implement aLow-complexity and low-leakage data retention SLEEP mode as illustrated in Fig.5. . One centralized NMOS sleep switch is shared by the gates in the master and slave stages of the sram FF. All of the devices along the critical path of the sram FF have low-|Vth|. The Clock-to-Q speed of the sram FF is therefore similar to a standard purely low-|Vth| flip-flop. The already existing sleep signal that is employed for ground gating is also used for controlling the data retention and restoration operations with the sram -FF. No extra control signals are required for the operation of the sram -FF. The sleep control and data transfer schemes of the sram FF are simple. The technique is effective for significantly reducing the leakage power consumption in idle sequential circuits[5].

The technique shown in Fig.5.6 (SRAM-FF) utilizes high-Vt NMOS pass transistor N1 for accessing a data retention cell (DRC) .The DRC is similar to a standard six-transistor SRAM cell used in the caches. One centralized (shared) NMOS sleep switch is utilized with the SRAM-FF. All of the devices along the critical path of the SRAM- FF have low-Vt. The speed of the SRAM-FF is, therefore, similar to a standard low-Vt FF .In the active mode, the sleep signal is set high, sleep transistor N1 is turned on. The feedback inverter (Ifb) and the transmission gate (TGcell) inside the DRC form the active mode feedback path of the slave latch. The circuit operation is similar to a standard low-Vt negative edge triggered FF. The data retention cell maintains the states of Node3 and Q whenever the clock is high (the slave stage is opaque) in the active mode. Whenever the clock transitions low, the feedback path within the DRC is cut-off. The last data sampled by the master stage edges of the clock. When the circuit is idle, the clock is gated high and the sleep signal transitions low The low-Vt gates in the FF are disconnected from the actual ground by cutting off the NMOS sleep switch. The access transistor N1 are cut-off, thereby disconnecting the DRC from the slave latch during the sleep mode. TG cell within the DRC is turned on since the clock is gated high. The data that was last sampled by the DRC is thereby maintained throughout the sleep mode. Note that the high-Vt cross-coupled inverters within the DRC are always connected to the actual VDD and GND (no VDD or Gnd gating in the sleep mode).The fig 5 shows the data retention digital TPS circuit with effective power consumption and area. These inverters are sized small and have high-Vt since these devices are not on the critical delay path of the FF. The sleep mode leakage power consumption of the SRAM-FF is thereby significantly reduced while maintaining the pre-sleep circuit state. At the end of the sleep mode, the sleep signal transitions high before the clock is enabled. SRAM-Node1 and SRAM-Node3 are connected to Node3 and Q through TG and N3, respectively. Depending on the pre-sleep data stored in the DRC, either Node3 (SRAM-Node1 = “0”) or Q (SRAM-Node3 = “0”) is discharged. After the data recovery is complete, the clock is enabled and the entire FF is reactivated. The steady-state voltages of all the nodes attached to the virtual linear VDD in the sleep mode in the gated-ground MTCMOS circuits. Node3 however can settle to an intermediate voltage lower than VDD since Node3 is isolated from the virtual ground line. Provided that SRAM-Node1 of the SRAM-FF stores a “1” during the sleep mode, Node3 voltage does not rise all the way up to VDD due to the Vt drop across TG during the data recovery operation at the end of the idle mode. Therefore, the low-Vt inverter (Is) in the slave latch of the SRAM-FF can be weakened during the first clock cycle of the active mode after a wake-up event. This Vt drop at Node3, however, typically does not produce a significant issue since the parallel feed-forward inverter (Ifr) within the DRC also supports the state of Q and drives the output load[6].

Sleep Signal Slew Rate Modulation Techniques under equal –Noise Constraints

Single phase sleep signal slew rate modulation, triple phase slew rate modulation, and stepwise Vgs MTCMOS circuits are evaluated in this section under an equal noise constraints. The sleep signal waveforms are tuned to suppress the peak ground bouncing noise to negligible level that is less than 2 mV with different MTCMOS circuit techniques. Peak noise voltages that are less than 2v are considered to be negligibly small in this paper[7].

The critical parameters of proffered implementation of TPS are listed in Table I.

Under equal noise constraints the main disadvantages of various previous techniques are for single phase sleep signal slew rate modulation is it increase the reactivation time and energy and also it is not suitable for the fast and energy efficient circuits as its reactivation delay is very high. For stepwise Vgs MTCMOS circuits are basically the methodology needed to choose the VX is not provided and the optimum Vx is varied with Vth of sleep transistor and also the process variation affect the performance.

The main problems of Triple phase sleep signal slew rate modulation using analog circuits are it consumes more power, it require more circuit area ,the single phases cannot tune individually and process variation would affect and also the deactivation time is very high. Also for various previous Data Retention technologies the data retention is not performed accurately by retention flip flops[8].

In the proposed system all the above mentioned problems are reduced[9]. There is a significant reduction in power consumption, the circuit area is reduced and process variation is not affecting the circuit. Effective data retention can be provided with the data retention technology introduced in this paper using the same sleep signal from the TPS modulator[10].

CONCLUSION

Sleep signal slew rate modulation techniques and data retention technology are explored in this paper for reducing mode transition noise in MTCMOS circuits. A triple-phase sleep signal slew rate modulation technique with a novel digital sleep signal generator with data retention is proposed. The new digital TPS technique enhances the overall electrical quality by 9.15×, 4.35×, and 1.21× as compared to previously published mixed-signal triple-phase, single-phase, and stepwise Vgs sleep signal slew rate modulated MTCMOS circuits, respectively, under an equal-noise constraint at the typical process corner in a UMC 80-nm CMOS technology. Furthermore, the digital TPS technique is identified as the most robust MTCMOS circuit technique among the MTCMOS circuits that are evaluated in this paper under both die-to die and within-die process parameter variations. The triple phase sleep signal slew rate modulation technique enhances the overall tolerance to process parameter fluctuations by up to 183.1× and 54.06× as compared to the single-phase and stepwise Vgs sleep signal slew rate modulation techniques, respectively, based on a comprehensive robustness metric.

REFERENCES

1. Abraham CG, Augustine L, Enhancement of tri model switch for low power VLSI application using HDL, International Journal of Emerging Technologies in Computational and Applied Sciences, 2012; 200-210.
2. Anis M, Areibi S, and Elmasry M, Design and optimization of multi-threshold CMOS (MTCMOS) circuits, IEEE Trans. Comput. AidedDesign Integr. Circuits Syst., 2003; 22(10): 1324–1242.
3. Henzler, Eireiner M, Berthold J, Georgakos, and Landsiedel DS, Activation technique for sleep-transistor circuits for reduced power supply noise, in Proc. IEEE Eur. SolidState Circuits Conf., 2006; 102–105.
4. Jiao and Kursun V, Ground bouncing noise aware combinational MTCMOS circuits, IEEE Trans. Circuits Syst. I, Reg. Papers, 2011;57(8):2053–2065.
5. Jiao and Kursun V, Sleep signal slew rate modulation for mode transition noise suppression in ground gated integrated circuits, in Proc. IEEE Int. SoC Conf., 2011; 365–370.
6. Jiao and Kursun V, Ground bouncing noise suppression techniques for data preserving sequential MTCMOS circuits, IEEE Trans. Very Large Scale Integr. (VLSI) Syst., 2011; 19(5): 763–773.
7. Jiao and Kursun V, Tri mode operation for noise reduction and data preservation in low leakage multi threshold CMOS circuits, in VLSISoC: Forward-Looking Trends in IC and System Design, J. L. Ayala, D. A. Atienza, and R. Reis, Eds. New York: Springer Verlag, 2012; 258–290.
8. Kurd, Bhamidipati S, Mozak C, Miller J, Mosalikanti P, Wilson T, El Husseini A, Neidengard M, Aly R, Nemani M, Chowdhury M,and Kumar R, A family of 32 nm IA processors,IEEE J. Solid StateCircuits, 2011; 46(1): 119–130.
9. KimSV, Stephen K, and Knebel DR, Understanding and minimizing ground bounce during mode transition of power gating structures, in Proc. Int. Symp. Low Power Electron. 2003; 22–25.
10. Mutoh, Douseki T, Matsuya Y, Aoki T, Shigematsu S, and Yamada J, 1-V power supply highspeed digital circuit technology," IEEEJ. Solid-State Circuits, 1995; 30(8): 847–854.

Table I: Parameters for Achieving Equal Noise with Sleep Signal Slew Rate Modulation Techniques

Circuit Technique	Parameters
Single Phase	Rise delay of sleep signal:43.40 ns
TPS	T1:.49v; T3:13.75ns; T3:900ps
Stepwise Vgs	Vx: 0.49V; T_{R_first}:1.9ns; T_{R_second} :1.1 ns; T_{relax} :10.76ns

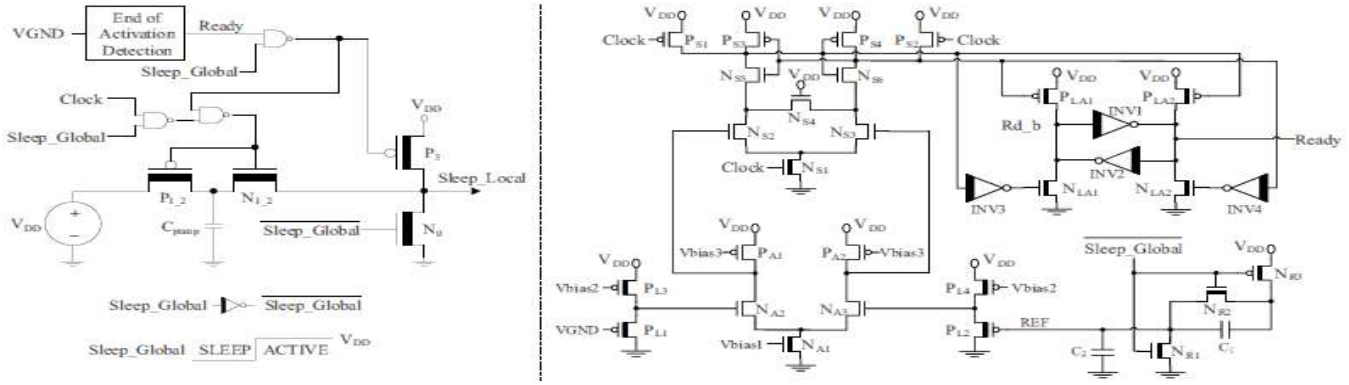

Figure 3: Analog triple phase sleep signal slew rate modulation

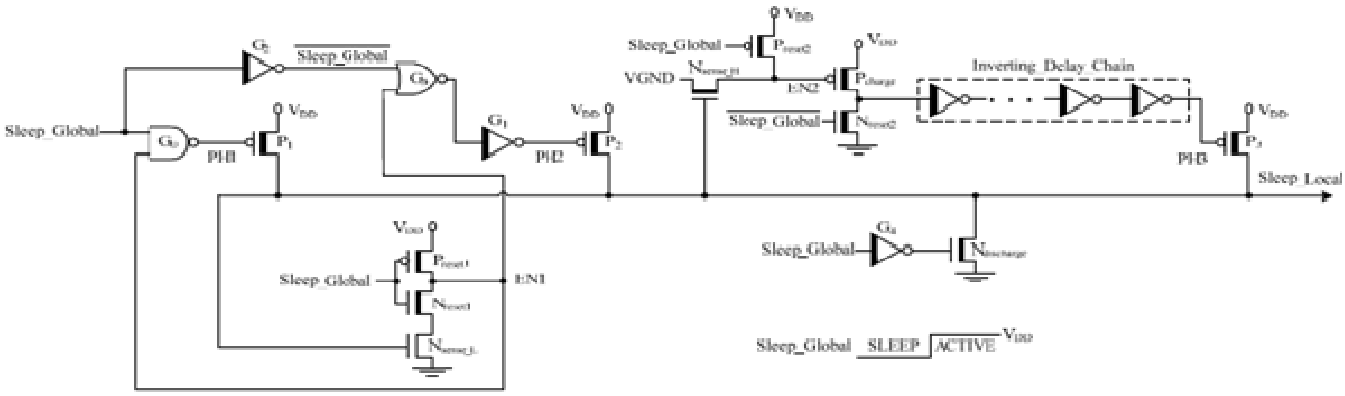

Figure 4: Digital Tripple phase Slew rate modulation

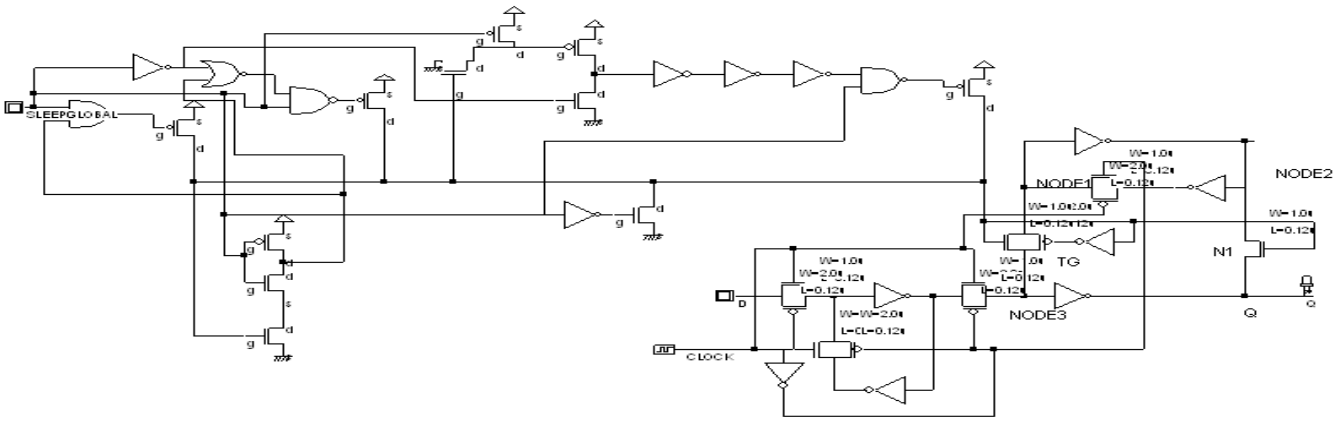

Figure 5: Digital TPS with Effective data retention

Source of support: Nil, Conflict of interest: None Declared