ISSN 2348-375X

Unique Journal of Engineering and Advanced Sciences

Available online: www.ujconline.net

Research Article

A HIGH PERFORMANCE SRAM ARRAY DESIGN USING COARSE GRAINED RECOVERY BOOSTING LOGIC

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Received: 05-03-2014; Revised: 04-04-2014; Accepted: 02-05-2014

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ABSTRACT

Negative bias temperature instability is an important reliability problem in electronic industry. The Static RAM based structures within the microprocessor are mostly susceptible to NBTI because one of the pMOS transistors in the memory cell always has an input of Zero. Here we propose a technique called Recovery Boosting that provides both pMOS transistors in the memory cell to be bring into the recovery model. Evaluate the circuit-level design of coarse and fine grained recovery boosting techniques. Then conduct an architecture-level verification of the performances and the reliability of using area-neutral designs of physical register files and the issue queues. T his shows that Coarse Grained Recovery Boosting provides significant improvement in speed while having very little impact on power consumptions and the performances.

Keywords: NBTI, Static RAM, DSCH, Micro wind, Physical register files, Issue queue

INTRODUCTION

The continued technology scaling of IC, the processors are becoming increasingly susceptible to hard error. Negative bias temperature instability is the one important hard error phenomenon which affects the lifetime of pMOS transistor. It occurs when a negative bias is applied at the gate of pMOS transistors. A interface trap is produced by this negative bias. It causes threshold voltage of the device increases. It will reduce the speed of the devices and also reduces the noise margin of the circuits; finally the circuit goes to damage. The interface traps can be eliminated by applying a logic input of "1" at the gate of the pMOS devices. This technique is known as recovery boosting. The static random access memory cells are mainly susceptible to hard error.

The Section II presents an overview of negative bias instability. The related work discuss on section III. The Section IV discusses the recovery boosting techniques and circuit-level designs, and the section V evaluation of the register files and the issue queue are given. The section IV experimental methodology used for the circuit-level evaluation is given. And finally the architecture-level evaluation is given.

What is Nagative Bias Instabiliy?

When the Si oxidization process, almost all of the Si atoms bond with oxygen and few of them bond with H. A negative bias is applied the relatively weak Si-H bonds get disturbes, this leading to the generation of interface traps. Interface traps cause the threshold voltage of the device increases, this in turn degrades the speed of the circuit.

Related work

Two basic approaches to mitigating negative bias instability: first reduce the stress on the pMOS transistor and second enhance the recovery time of Pmos.

Stress Reduction Techniques: The Srinivasan et al. estimate the MTTF based on the operating conditions and use dynamic reliability management to stay within the reliability budgets

Recovery-Enhancement Techniques: The Abella et al. propose to feed specific bit patterns into the devices to increase the recovery time for pMOS transistors in logic structures during idle periods and balance the degradation of the pMOS devices in SRAM-based memory structures when they hold invalid data's.

Concepts Of Recovery Boosting

We can discuss before about recovery boosting techniques, 1st review the design and operation of a conventional 6-transistor SRAM cells. The 6T cell is given in Fig. 1(a). The cell is composed of a word line , bit lines , 2 cross-coupled inverters and 2 access transistors N0,N1. Inverters store one bit. Three basic operations: read, write and hold. The cell is accessed by raising WL to one. It activates the access transistors No& N1 and that connects the cell to the bit lines

BL & BLB .The cells are not selected for read or write operations, we expect that cell is in hold state.

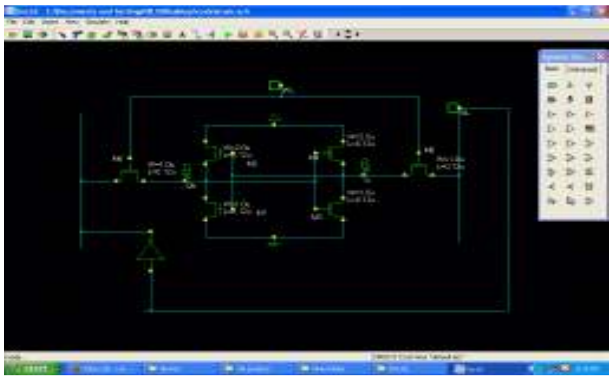

Figure 1: Conventional 6T SRAM Cell

The SRAM cell has cross-coupled inverters i0& i1, so each inverter charges the gate of the other. However, all time one of the pmos has an input value of zero. Goal of recovery enhancement is apply logic one to the input of pmos transistor. Basic idea of recovery boosting is to raise the node voltages of a memory cell. It can be achieved by raising the ground voltage.

Fine-Grained Recovery boosting techniques

The normal operating mode, bit lines is shared by all the memory cells in a given column. So, even those memory cells that are not performing read & write operation. Bit line transitions not affecting the normal operation of the ordinary the cells. To perform recovery boosting, bit lines of the cell want to be raised to high. So, need to be able to isolate the bit lines that are in the recovery boost mode.

We can provide this isolations by extending the memory cell with connections to the rail of an adjoining row or column via two pMOS access transistors. The modified SRAM cell used for controlling individual entries for both normal mode and the recovery boost mode is shown in above section. In modified cell the CR signal used for switch between the normal mode and recovery mode. CR =1 the cell goes to recovery boost mode, moreover raise the ground voltage to 1, two extra pMOS devices are also turned on. With these connections we can put the cell in to recovery mode individually.

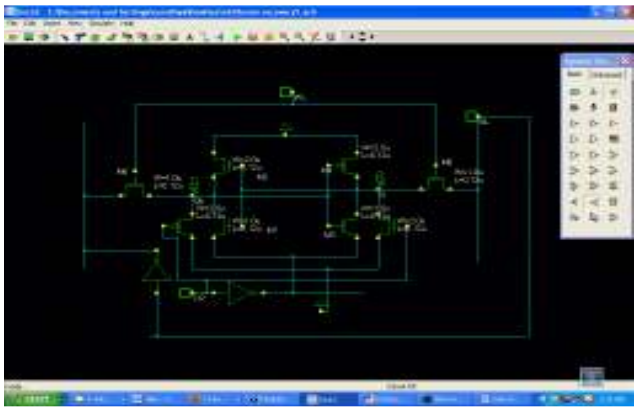

Figure 2: Modified SRAM cell with connection to the Vdd rail of an adjoining row

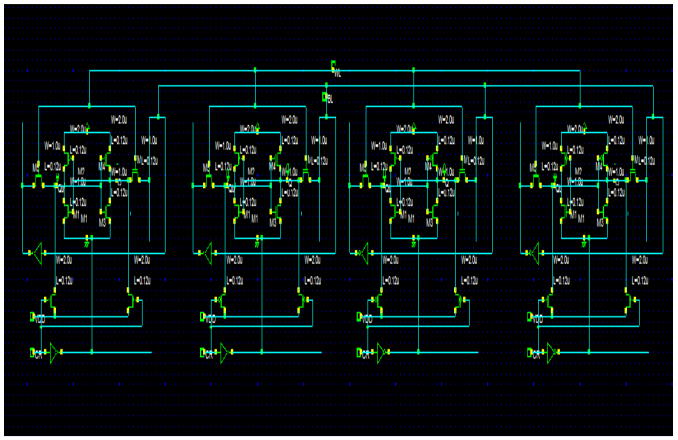

Figure 3: Fine grained Recovery boosting in SRAM arrays.

These devices do not effect performance strongly but it delay the transition between the normal mode to recovery boost mode. Not only is that area critical in this boosting technique.

Coarse-Grained Recovery boosting techniques

This approach the SRAM cell design has shown in Fig. 5 instead of the one control for fine-grained. A single control signal uses for the entire array into the . Control signal CR with a value of "0" raises the ground connection of each entry.

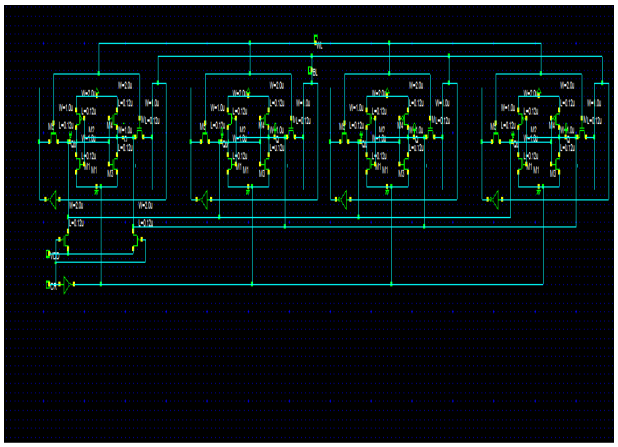

Figure 4: Coarse grained Recovery boosting in SRAM array.

Designing Micro Architectural Structures That Support Recovery Boosting

We have discussed the basics of recovery boosting, next is designing of SRAM-based micro architectural structures that uses this technique to prevent NBTI. Here, present and evaluate the circuit-level design of two large SRAM-based structures such as physical register file and the issue queue.

Physical Register File

A 32-bit microprocessor has (mostly) 32-bit registers internally. Here construct a 4x4 "register file" comprising registers R0, R1, R2 and R3. A register file comprises a decoder which chooses a destination register and a multiplexer to direct the outputs of any register through to the data output lines. The decoder select lines may then be viewed as the destination "address" and the multiplexer select lines as the source "address".

The four registers R0, R1, R2 and R3 in the diagram below are to be implemented using the VHDL code . Each register comprises 4 static RAM cell. Each register has a 4-bit input data and a 4 bit output data. In this project replace the static RAM by modified static RAM and evaluate the performance of the register file.

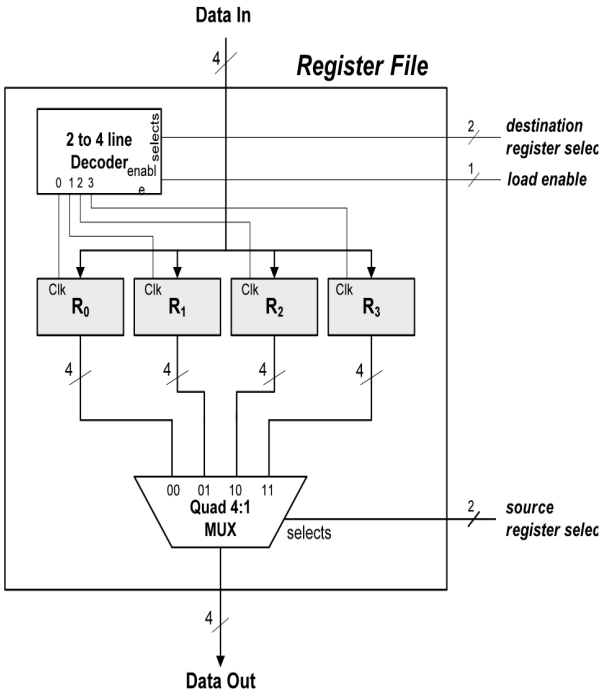

Figure 5: Physical register file

Issue Queue

The microprocessor executes a program first it fetching the instruction from memory next executing the same. Normally the processor execution speed is more than the memory access speed. Prefetch the next instructions in a separate buffer by using issue queue when the microprocessor is executing the current instruction.

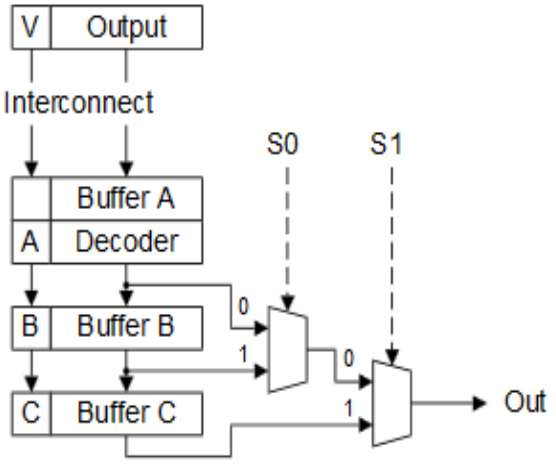

Figure 6: Issue queue.

The buffer is a physical memory used for store data temporarily. Typically, the buffers comprises of static RAM cell .The proposed method is to replace the static RAM cell with modified SRAM cell. The instructions written in the buffer A decodes as soon as it arrives by decode The buffers B and C used for receive the instruction which is decoded version of buffer A instruction.

RESULTS

Circuit-Level Simulation Results

We perform simulation using Micro wind 3.1 circuit simulators to verify the functionality of conventional cell and modified cell. Also verify the functionality of fine grained and coarse grained recovery boosting. Calculate the power consumption.

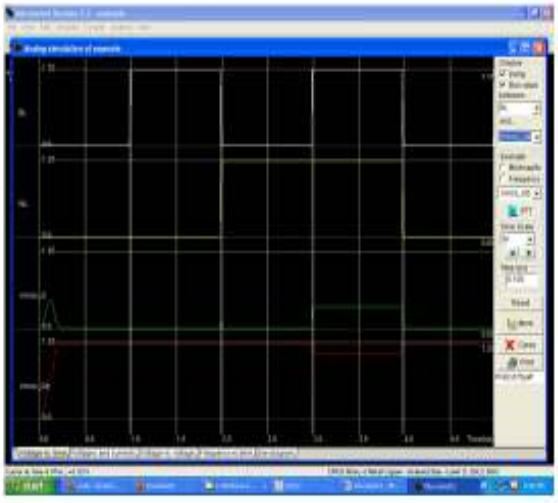

Figure 7: Waveform of conventional 6T SRAM Cell.

When WL=1, BL=1 the output node Q will be high. When WL=1, BL=0 the output node Q will be low. Power P=92.015015u w

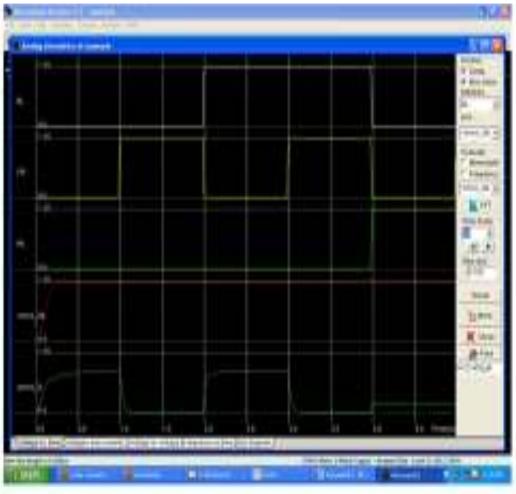

Figure 8: Waveform of SRAM cell support partial recovery

CR =1, SRAM cell can perform normal mode. CR=0, the cell is in recovery mode. Power P=72.453015u w

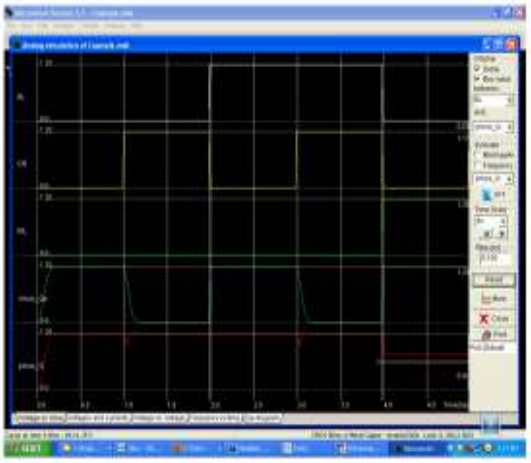

Figure 9: Waveform of modified SRAM cell.

To provide isolation extend the memory cell with connections to the rail an adjoining row or column via two PMOS access devices. So powers will more than other. Power P = 0.153mw.

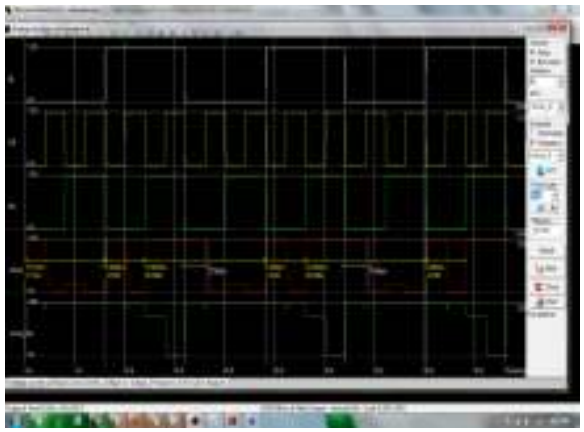

Figure 10: Waveform of Modified cell with combined (coarse grained).P=0.380mw.

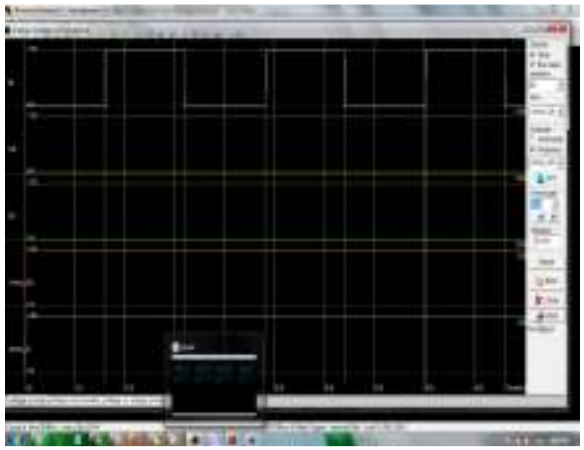

Figure 11: Waveform of modified cell (Fine grained).P=4.590uw

Architecture-Level Simulation Results

Area-neutral designs of physical register file and issue queue structures can provide significant improvements with very little impact on power and negligible loss in performance.

CONCLUSION

NBTI is the most important problem in the microprocessors .The SRAM based structures is mostly vulnerable to NBTI. In this paper, we proposed recovery boosting technique that permits both pMOS in the cell into the recovery mode. We show how fine-grained and coarse grained recovery boosting works. Then show how coarse grained design works with the physical register file and issue queue.

ACKNOWLEDGEMENT

The authors would like to thank Prof. H.S. Divakara Murthy, Dean & HOD of ECE department for his constructive comments and suggestions.

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Source of support: Nil, Conflict of interest: None Declared