ISSN 2348-375X

Unique Journal of Engineering and Advanced Sciences

Available online: www.ujconline.net

Research Article

DUAL DYNAMIC EDGE TRIGGERED LOW POWER FLIP-FLOP FEATURING ELM

Varuna RTV[1*], Prabhakaran G[2], Marimuthu CN[3]

[1]PG Student, Department of Electronics and Communication Engineering,Nandha Engineering College, Erode-638052, Tamil Nadu, India
[2]Assistant Professor, Department of Electronics and Communication Engineering,Nandha Engineering College, Erode-638052, Tamil Nadu, India
[3]Dean, Department of Electronics and Communication Engineering, Nandha Engineering College, Erode-638052, Tamil Nadu, India

Received: 30-12-2013; Revised: 29-01-2014; Accepted: 28-02-2014

*Corresponding Author: **Varuna R.T.V** Email: varuvais@gmail.com

ABSTRACT

In this paper, a modified Dual Dynamic Flip-Flop by using edge triggering with a novel embedded logic module is introduced. It presents speed efficient method to incorporate complex logic functions into the flip-flop with small delay penalty. The proposed design reduces the power consumption up to 20% compared to the conventional flip-flops. The aim is to reduce the large delay, leakage power and to reduce the power dissipation by reducing the precharge capacitance. Also, the design is compared with other state-of-the-art designs. A high speed ring counter using digital CMOS gate logic components by the DDFF structure is also designed which is well suited for modern high performance circuits. Finally simulation results are tested using TSPICE.

Keywords: Edge triggering, embedded logic module, flip-Flop, power dissipation, delay penalty.

INTRODUCTION

During the desktop PC design era, VLSI design efforts have focused primarily on optimizing speed to realize real time functions. With the growing trend towards portable computing and wireless communication, the need for low power has became as important as performance and area. Based on the comparison of the power breakdown for different elements in VLSI chips, latches and flip-flops are the major source of the power consumption in synchronous system. Therefore study on low-power and high performance latches and flip-flops is inexorable.

Flip-Flops (FFs) and latches are the basic storage elements used extensively in all kinds of digital designs. In particular, digital designs nowadays often adopt intensive pipelining techniques and employ many FF-rich modules. In the past decades, many works has been dedicated to improve the performance of the flip-flops[4,8]. Several hybrid flip-flop designs have been proposed to reduce the power and delay[14-16]. The Hybrid Latch Flip-Flop[8] is a high performance flip-flop implementing a new mechanism of performing flip-flop functionality based on generating explicit transparency window where the transition is allowed. This approach greatly reduces the complexity of the locking mechanism resulting in small delay and small area[7]. This flip-flop falls under hybrid category which has impressive delay property and can have negative setup time.

Semi Dynamic Flip-Flop (SDFF)[4] is a combination of static and dynamic circuits. They are called as hybrid structures because they consist of a dynamic frontend and a static output. It has the capability of incorporating logic very efficiently, because unlike the true single phase latch (TSPC)[14], only one transistor is driven by the data input.

A flip-flop architecture which was introduced, named Cross Charge Control Flip-Flop (XCFF)[3] has considerable advantages over SDFF and HLFF in both power and speed. Since only one of the two dynamic nodes is switched during one CLK cycle, the total power consumption is considerably reduced without any degradation in speed. Also XCFF has a comparatively lower CLK driving load.

A recent paper [1] introduced a new dual dynamic node hybrid flip-flop (DDFF) and a novel embedded logic module (DDFF-ELM) based on DDFF. It has a split dynamic node structure to separately drive the output pull-up and pull down transistors. Despite of incorporating complex logic functions into the flip-flop, this structure has some drawbacks. It has a larger delay penalty and more number of inverter gates is required to trigger the flip-flop.

In this paper, we propose a modified Dual Dynamic Flip-Flop by using edge triggering which reduces the power consumption compared to the above flip-flop architectures. The performance of modern high performance flip-flops are compared with the modified structure and the power consumption is estimated using tanner tool. The new design is

free from unwanted transitions and it has reduced switching activity. It uses an embedded logic module which incorporates complex function into the flip-flop with small delay penalty. The proposed design has the power reduction of 20% compared to the other flip-flops.

ANALYSIS OF EXISTING FLIP-FLOP ARCHITECTURES

In the past decades, a large number of latches and flip-flops introduced can be grouped under the static and dynamic design styles. HLFF as shown in Figure 1 is a static, single edge-triggered FF which consumes more power[2]. Existence of redundant transition in internal nodes of HLFF indicates more power consumption. This structure is basically a level sensitive latch which is clocked with an internally generated sharp pulse. This sharp pulse is generated at the positive edge of the clock using clock and delayed version of clock. The major advantage is its soft-edge property and its simplicity. The major disadvantage is that it not suitable for low power application, since its power consumption limits it utilization.

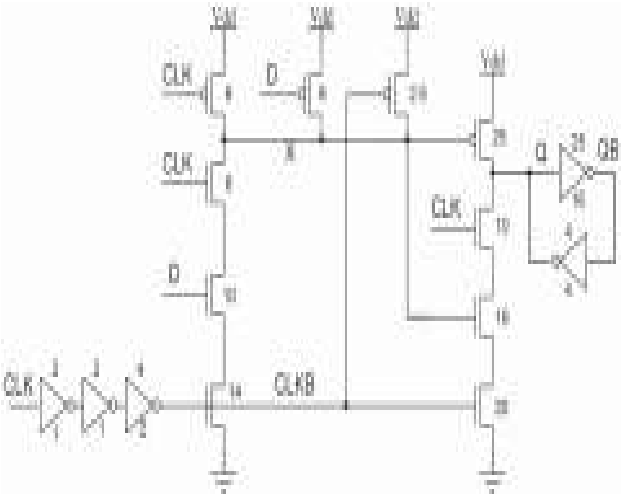

Figure 1: Hybrid Latch Flip-Flop

In the Cross Charge Control Flip-Flop (XCFF) [3] as shown in Figure 2, it uses a split-dynamic node to reduce the precharge capacitance, which is one of the most important reasons for the large power consumption in most of the conventional designs. It reduces the power dissipation by splitting the dynamic node into two, each one separately driving the output pull-up and pull-down transistors. despite having a single data-driven transistor, embedding logic to XCFF is not very efficient due to the susceptibility to charge sharing at the internal dynamic nodes. Power consumption is reduced compared to HLFF and SDFF. Redundant power dissipation occurs as the data does not switch for more than one clock.

The DDFF architecture [1] is shown in the Figure 3.It consists of two nodes. Node X1is pseudo-dynamic, with a weak inverter acting as a keeper, whereas, compared to the XCFF, in this architecture node X2 is purely dynamic. An unconditional shutoff mechanism is provided at the frontend instead of the conditional one in XCFF.

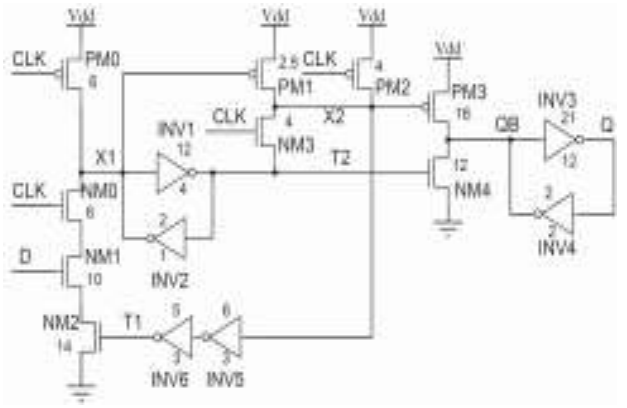

Figure 2: Cross Charge Control Flip-Flop

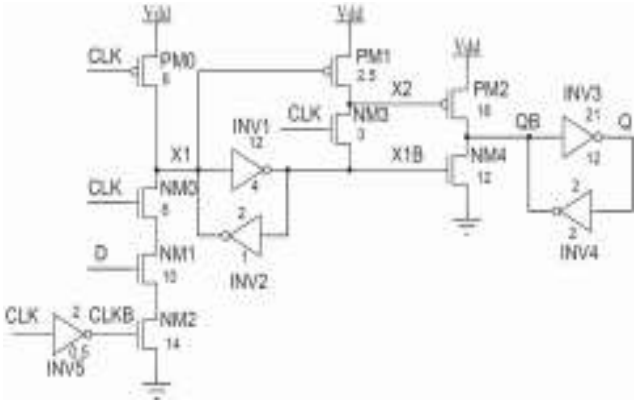

Figure 3: Dual Dynamic Flip-Flop

PROPOSED MODIFIED DDFF ARCHITECTURE

Various functions have been embedded into the proposed design to analyze the performance of the structure in terms of power and speed. In the existing systems more number of gates are used which increases the delay and area. The power consumption is reduced in the modified system by reducing the number of gates and by using edge triggering. This further reduces the power consumption since it halves the frequency. The delay is also reduced compared to the above architectures. The modified structure is shown in Figure 4.

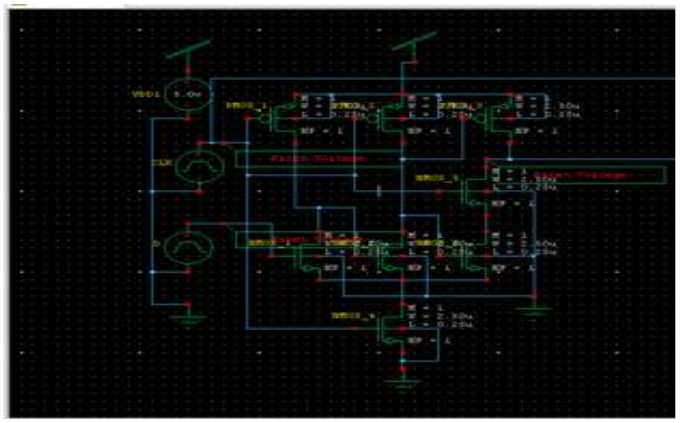

Figure 4: Modified DDFF with edge triggering

The operation of the flip-flop can be divided into two phases: i) the evaluation phase, when CLK is high, and ii) the precharge phase, when CLK is low. If D is high, node X1 is discharged through NM0-2. This switches the state of the cross coupled inverter pair INV1-2 causing node X1B to go high and output QB to discharge through NM4. Thus, node X2 is held high throughout the evaluation period by the PMOS transistor PM1. As the CLK falls low, the circuit enters the precharge phase and node X1 is pulled high through PM0, switching the state of INV1-2. During this period node X2 is not actively driven by any transistor, it stores the charge dynamically.

If D is zero prior to the overlap period, node X1 remains high and node X2 is pulled low through NM3 as the CLK goes high. Thus, node QB is charged high through PM2 and NM4 is held off. At the end of the evaluation phase, as the CLK falls low, node X1 remains high and X2 stores the charge dynamically.

PERFORMANCE ANALYSIS

To analyse the performance of modified DDFF architecture a ring counter is designed. It highlights the performance of the proposed flip-flop architecture. The reason for considering a counter is that the data activity at each bit position is known. The basic structure of a ring counter is shown in Figure 5.

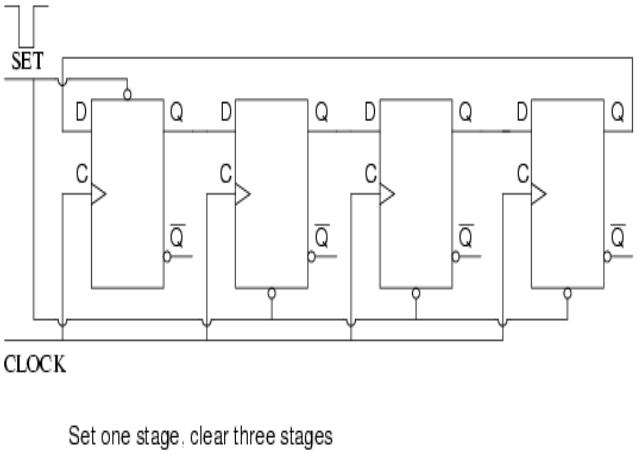

Figure 5: Ring counter

A ring counter is a type of counter composed of a type circular shift register. The output of the last shift register is fed to the input of the first register. The propagation delay will be a constant regardless of the number of bits in the code.

SIMULATION RESULTS

Tanner EDA is a leading provider of easy-to-use, PC-based electronic based design automation (EDA) software solutions for the design, layout and verification of analog/mixed-signal integrated circuits, ASICs and MEMS. The result is simulated in TSPICE platform

XCFF Architecture

The power consumption is less than the hybrid and semi dynamic flip-flops. The effect of charge sharing becomes uncontrollably large when complex functions are embedded into the design. The schematic diagram is shown in Figure 6.

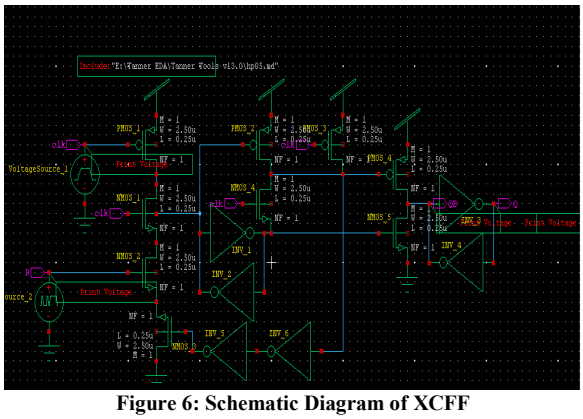

Figure 6: Schematic Diagram of XCFF

DDFF Architecture

The schematic diagram is shown in Figure 7. The power consumption is low compared to the other conventional flip-flops. There is larger number of inverter gates to trigger the flip-flop. Therefore there is large delay.

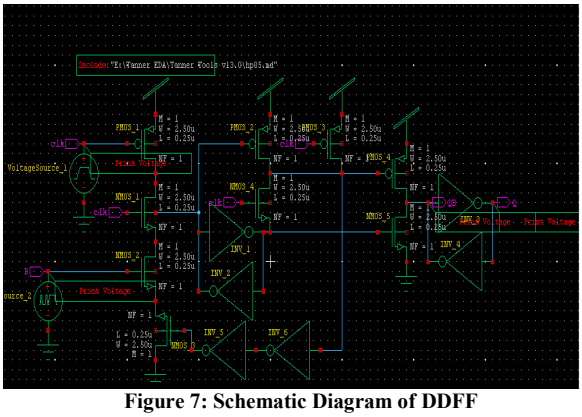

Figure 7: Schematic Diagram of DDFF

Modified DDFF Architecture(proposed)

In the proposed structure minimum number of gates is used which reduces the power consumption compared to the existing architectures. The edge triggering is provided by the NMOS as shown in Figure 8.

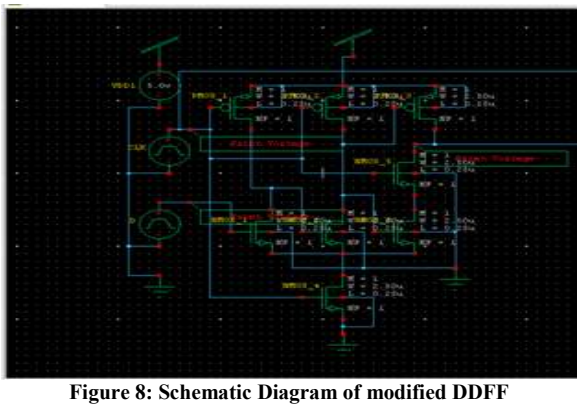

Figure 8: Schematic Diagram of modified DDFF

Ring Counter (proposed)

A 4-bit ring counter is designed using the dual dynamic flip-flop. With the initial register values of 1000, the repeating pattern is 1000, 0100, 0010, 0001, 1000...The schematic diagram is shown in Figure9.

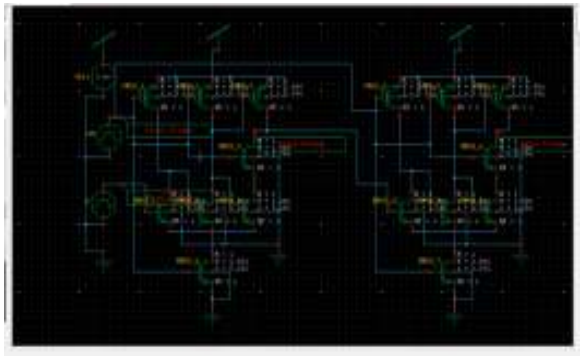

Figure 9: Schematic Diagram of Ring Counter

The power comparison is shown in Table 1.The modified DDFF structure has the reduced power consumption compared to the other structures.

PARAMETERS OF FLIP-FLOP	HLFF	SDFF	XCFF	DDFF	Modified DDFF (proposed)
Number of transistors	20	23	21	18	8
Average Power (W)	0.5294	0.6775	0.6576	0.5644	0.4201
Maximum Power (mW)	1.4012	0.3730	0.6272	0.3531	0.2922
Minimum Power (mW)	0.5011	2.3194	1.213	0.1692	0.1422

CONCLUSION

In this paper, a modified DDFF with edge triggering were proposed for low power application. A scalable high-speed counter using digital CMOS gate logic components were designed to highlight the performance of the flip-flop. Our counter design logic is comprised of CMOS circuits for DFF by the proposed method of DDFF structure. The proposed design successfully simplifies the control logic and PMOS and NMOS transistor alone serves the purposes of both mode select and counter excitation logic. The circuit simplicity leads to a shorter critical path and reduced power consumption. The power consumption is reduced to 20% than the existing systems. Post layout simulation results proved its advantages in power and speed against previous designs.

REFERENCES

1. KalarikkalAbsel, Lijo Manuel, R.K.Kavitha. Low Power Dual Dynamic Node Pulsed Flip-Flop featuring efficient embedded logic. 2013; 21(9).
2. Hansson M, Alvandpour A. Comparative analysis of process variation impact on flip-flop power-performance," in Proc. IEEE Int.Symp. Circuits Syst. 2007; 3744.
3. Hirata AK, Nakanishi K, Nozoe M, Miyoshi A. The cross charge control flip-flop: A low-power and high-speed flip-flop suitable for mobile application SoCs, in Proc. Symp. VLSI Circuits Dig. Tech.Papers. 2005; 306.
4. KlassF. Semi-dynamic and dynamic flip-flops with embedded logic,in Proc. Symp. VLSI Circuits Dig. Tech. Papers, Honolulu. 1998; 108.
5. Ma A, Asanovic K. A double-pulsed set-conditional-reset flipflop,Laboratory for Computer Science, Massachusetts Inst. Technology, Cambridge, Tech. Rep. MIT-LCS-TR-844. 2002.
6. Mahmoodi H, Tirumalashetty V, Cooke M,Roy K. Ultra low power clocking scheme using energy recovery and clock gating," IEEETrans. Very Large Scale Integr. (VLSI) Syst. 2009; 17(1): 33.
7. Nedovic N, Oklobdzija VG. Hybrid latch flip-flop with improved power efficiency, in Proc. Symp. Integr. Circuits Syst. Design. 2002; 11.
8. Patrovi H, Burd R, Salim U, Weber F, DiGregorio L, Drape D. Flow-through latch and edge-triggered flip-flop hybrid elements," in Proc. IEEE ISSCC Dig. Tech. Papers. 1996; 138.
9. Rabaey JM, Chandrakasan A, Nikolic B. Digital IntegratedCircuits: A Design Perspective, 2nd ed. Englewood Cliffs, NJ: Prentice-Hall. 2003.
10. Rasouli SH, Khademzadeh A, Afzali-Kusha A, NouraniM. Low-power single- and double-edge-triggered flip-flops for high-speed applications, Proc. Inst. Elect. Eng. Circuits Devices Syst. 2005; 152(2): 118.
11. SarbisheiO,Maymandi-NejadM. Power-delay efficient overlap based charge-sharing free pseudo-dynamic D flip-flops, in Proc. IEEEInt. Symp. Circuits Syst. 2007; 637.
12. Sarbishei O,Maymandi-Nejad M. A novel overlap-based logic cell: An efficient implementation of flip–flops with embedded logic," IEEE Trans. Very Large Scale Integr. (VLSI) Syst. 2010; 18(2): 222.
13. Stojanovic V, OklobdzijaV. Comparative analysis of master slave latches and flip-flops for high-performance and low-power systems,"IEEE J. Solid-State Circuits. 1999; 34(4): 536.
14. Teh CK, Hamada M, Fujita T, Hara H, Ikumi N, Oowaki Y. Conditional data mapping flip-flops for low-power and high performance systems, IEEE Trans.Very Large Scale Integr. (VLSI) Syst. 2006; 14(12): 1379.
15. YuanJ, Svensson C. New single-clock CMOS latches and flip-flops with improved speed and power savings, IEEE J. Solid-State Circuits. 1997; 32(1): 62.
16. Zhao P, Darwish TK, BayoumiMA. High-performance and low-power conditional discharge flip-flop, IEEE Trans. VeryLarge Scale Integr. (VLSI) Syst. 2004; 12(5): 477.

Source of support: Nil, Conflict of interest: None Declared