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Research Article

DESIGN OF DOUBLE TAIL COMPARATOR FOR ANALOG TO DIGITAL CONVERSION

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ABSTRACT

Comparator plays a major role on the overall performance of high speed analog to digital converters. A clocked comparator has to find out whether the input signal is high or low at every clock cycle. Since it acts as interface between the analog and digital signal, the accuracy is given by its input referred offset voltage, essential for the resolution of high performance ADC's. Based on the analysis of working of two different types of comparator it's found that time taken for the capacitive charging and discharging is found high. So in order to reduce the circuit delay we are going to use two tail transistor , as one at the top vdd and other at bottom vss, by including this transistor positive feedback during regeneration is strengthened, which result in remarkable reduce in delay time. In the proposed comparator, power consumption and delay are reduced significantly. The 0.18-µm CMOS technology post layout simulation confirms the result.

Keywords: Conventional Dynamic Comparator, Analog to Digital Converters, Double Tail Comparator, Regenerative Comparator.

INTRODUCTION

The high speed Analog To Digital Converters (ADC's) are being has continuously pushed towards their performance limits as technology scales down and system specification become more challenging. In "wearable computing" appliances the ultra-low power consumption requirement originating and also increase the sampling rates in modern communication systems among the rest, make challenge on ADC design. As comparator are most probably second most widely used electronic component after operational amplifier in this era, so it is used in abundance in A/D converters[1-4]. A comparator is also known as 1 bit analog to digital converter. In analog to digital conversion process, it is necessary to first sample input (using sample and hold circuit) and is applied to a combination of comparators to determine the digital equivalent of the analog signal. The conversion speed of the comparator is controlled by the decision making response time of the comparator. The ultra-deep sub micrometer (UDSM) CMOS technology suffers from low supply voltage especially when considering the fact that threshold voltages of the devices have not been scaled at the same pace as the supply voltage of the modern CMOS process[19]. So designing high speed comparator is more challenging when supply voltage is smaller. So to achieve high speed, large transistor are required to compensate the reduction of supply voltage, which also lead to more die area and power is needed. The low-voltage operation results in limited common mode input range, which is more important for many high speed ADC architectures, such as flash ADC's[5-9].

This paper is organized as follows. The section II investigates the operation of conventional dynamic comparator and its result. Section III gives the operation and result of double tail comparator. Section IV gives the operation of proposed double tail comparator and its result. Section V presents, list of comparison between different types of comparator. Finally, in section VI some conclusions are drawn[10-13].

Conventional Dynamic Comparator

The conventional dynamic comparators have found wide applications in many high speeds ADC's since they can make fast decisions due to the strong positive feedback in the regenerative latch[12]. Many comprehensive analyses have been presented in recent years, which investigate the performance of comparator in different aspects. The architecture of the conventional dynamic comparator is shown in the figure.1.

The operation of the comparator is as follows. Start condition will happen when CLK=0(low), which leads to Mtail off and other transistor M7 & M8 makes both the output nodes Outp

and Outn to VDD [1]. When CLK=VDD(high), transistor M7 and M8 ear off and Mtail is on. Output voltages which were pre- charged to high voltage will start to discharge with different rates depending on the corresponding input voltage (INN/INP)[14].

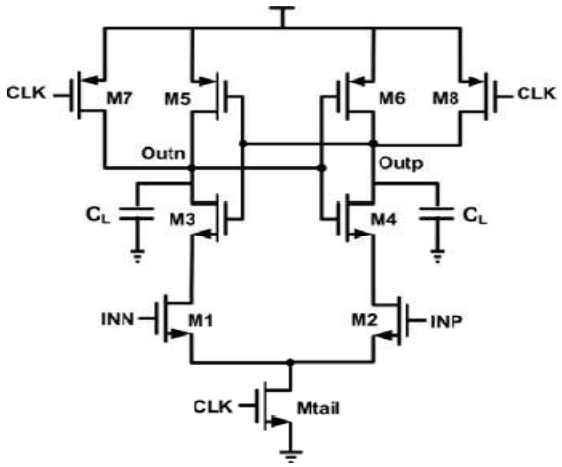

Figure 1: Architecture of conventional dynamic comparator.

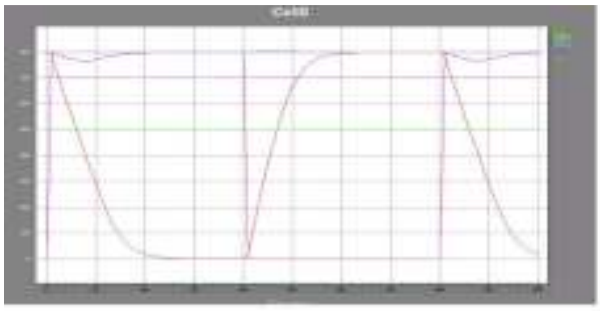

Figure 2: Waveform of conventional dynamic comparator.

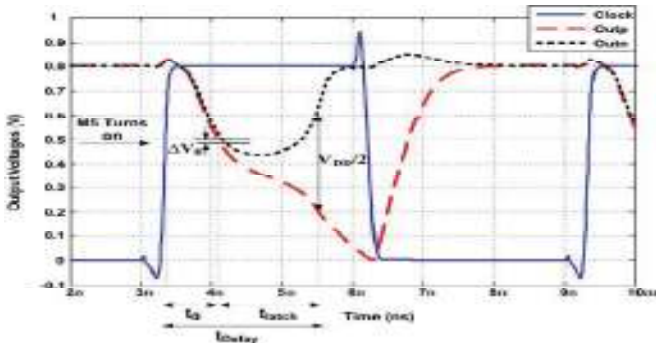

Figure 3: Transient simulation of convention dynamic comparator for delay calculation.

Assuming the case where VINN > VINP, Outn discharges faster than Outp, hence when Outn (discharged by transistor M1 drain current), falls down to VDD --|Vthn| before Outp (discharged by transistor M2 drain current) the corresponding pMOS transistor (M6) will turn on initiating latch regeneration by inverters(M3, M5 and M4, M6). Thus, Outp pulls to VDD and Outn discharges to ground. If VINN < VINP, the circuit works vice versa. As shown in the figure 2. Figure 3 shows the delay analysis of the conventional dynamic comparator output, from that we can calculate *t*0 delay, which represent the capacitive discharge of the load capacitance CL until the first P-channel transistor (M5/M6) turns on. And another tlatch delay occur is due to cross coupled inverter[15].

This structure has the advantages of high input impedance[13], rail-to-rail output swing[14], no static power consumption[15] and good robustness against noise[16].

Conventional Double Tail Comparator

The systematic diagram of conventional comparator is shown below in figure 4.

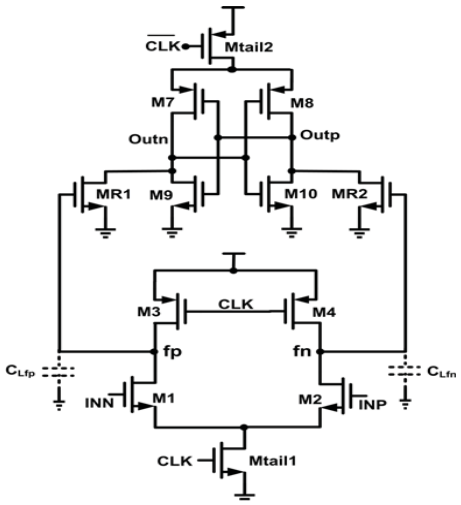

Figure 4: Architecture of conventional comparator.

The operation of this comparator is as follows (see Fig. 4)[11]. During reset phase (CLK = 0, *M*tail1, and *M*tail2 are off), transistors *M*3-*M*4 pre-charge fn and fp nodes to *V*DD, which in turn causes transistors *M*R1 and *M*R2 to discharge the output nodes to ground. During decision-making phase (CLK = *V*DD, *M*tail1 and *M*tail2 turn on), *M*3-*M*4 turn off and voltages at nodes fn and fp start to drop with the rate defined by *I*Mtail1/*C*fn(p) and on top of this, an input-dependent differential voltage Δ*V*fn(p) will build up[10].

Similar to the conventional dynamic comparator, the delay of this comparator comprises two main parts, *t*0 and *t*latch. The delay *t*0 represents the capacitive charging of the load capacitance *CL*out (at the latch stage output nodes, Out*n* and Out*p*) until the first n-channel transistor (*M*9/*M*10) turns on, after which the latch regeneration starts; thus *t*0 is obtained[19].

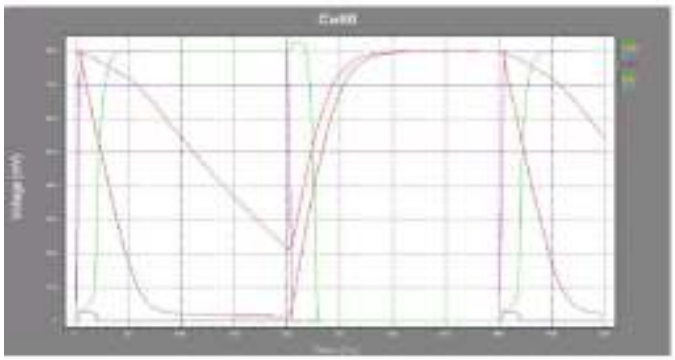

Figure 5: Waveform of conventional double tail comparator.

Proposed Comparator

The schematic architecture of proposed comparator is shown below in Figure 6. . The main idea of the proposed comparator is to increase ΔVfn/fp in order to increase the latch regeneration speed. For this purpose, two control transistors (*M*c1 and *M*c2) have been added to the first stage in parallel to *M*3/*M*4 transistors but in a cross-coupled manner

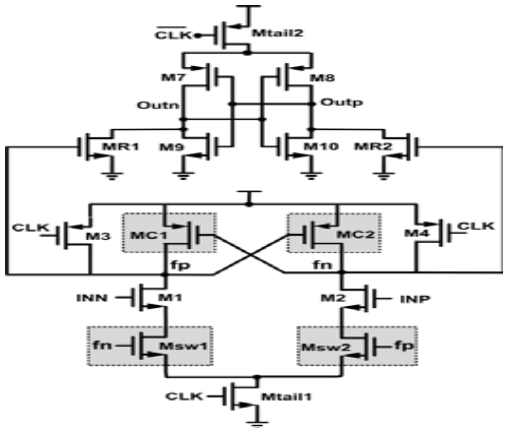

Figure 6 (a): Architecture of proposed comparator.

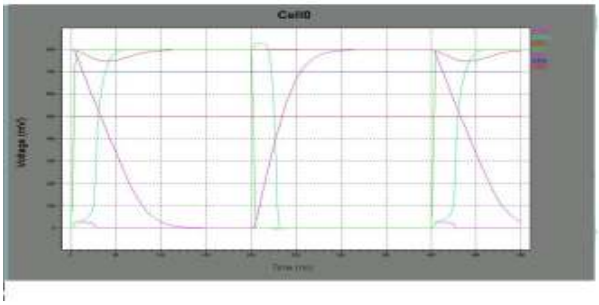

Figure 6 (b): Waveform of proposed comparator

The operation of the proposed comparator is as follows (see Fig. 6)[1]. During reset phase (CLK = 0, *M*tail1 and *M*tail2 are off, avoiding static power), *M*3 and *M*4 pulls both fn and fp nodes to *V*DD, hence transistor *M*c1 and *M*c2 are cut off. Intermediate stage transistors, *M*R1 and *M*R2, reset both latch outputs to ground During decision-making phase (CLK = *V*DD, *M*tail1, and *M*tail2 are on), transistors *M*3 and *M*4 turn off. Furthermore, at the beginning of this phase, the control transistors are still off (since fn and fp are about *V*DD)[3].

Thus, fn and fp start to drop with different rates according to the input voltages. Suppose *V*INP > *V*INN, thus fn drops faster than fp, (since *M*2 provides more current than *M*1)

Comparison between different types of comparators.

By using the 180-nm technology with supply voltage of 0.8 v we get the delay and power consumption as follows

Table 1: Comparison in working of different types of comparator

Process	Delay	Power Consumption
Single Tail Comparator	7 µw	66ns
Conventional	15 µw	7.5ns
Proposed	12 µw	7.4ns

CONCLUSION

Thus two basic structure of comparator where analyzed, based on that a new type of comparator was designed with low power and low voltage, which has improved the performance of comparator. The post layout simulation result in 180nm CMOS technology confirmed that the delay and power consumption of the comparator is reduced to great extent.

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